



United States Department of Commerce  
Technology Administration  
National Institute of Standards and Technology



NIST  
PUBLICATIONS

## ***NIST Technical Note 1295***

---

# ***Initial Graphics Exchange Specification Hybrid Microcircuit Application Protocol***

***Curtis Parks, Roger McCollough, Charles Azu,  
Larry Savage, Patrick Toomey, and Thomas Makoski***

---

~~QC~~  
100  
.U5753  
#1295  
1993

**T**he National Institute of Standards and Technology was established in 1988 by Congress to “assist industry in the development of technology . . . needed to improve product quality, to modernize manufacturing processes, to ensure product reliability . . . and to facilitate rapid commercialization . . . of products based on new scientific discoveries.”

NIST, originally founded as the National Bureau of Standards in 1901, works to strengthen U.S. industry's competitiveness; advance science and engineering; and improve public health, safety, and the environment. One of the agency's basic functions is to develop, maintain, and retain custody of the national standards of measurement, and provide the means and methods for comparing standards used in science, engineering, manufacturing, commerce, industry, and education with the standards adopted or recognized by the Federal Government.

As an agency of the U.S. Commerce Department's Technology Administration, NIST conducts basic and applied research in the physical sciences and engineering and performs related services. The Institute does generic and precompetitive work on new and advanced technologies. NIST's research facilities are located at Gaithersburg, MD 20899, and at Boulder, CO 80303. Major technical operating units and their principal activities are listed below. For more information contact the Public Inquiries Desk, 301-975-3058.

---

### **Technology Services**

- Manufacturing Technology Centers Program
- Standards Services
- Technology Commercialization
- Measurement Services
- Technology Evaluation and Assessment
- Information Services

### **Electronics and Electrical Engineering Laboratory**

- Microelectronics
- Law Enforcement Standards
- Electricity
- Semiconductor Electronics
- Electromagnetic Fields<sup>1</sup>
- Electromagnetic Technology<sup>1</sup>

### **Chemical Science and Technology Laboratory**

- Biotechnology
- Chemical Engineering<sup>1</sup>
- Chemical Kinetics and Thermodynamics
- Inorganic Analytical Research
- Organic Analytical Research
- Process Measurements
- Surface and Microanalysis Science
- Thermophysics<sup>2</sup>

### **Physics Laboratory**

- Electron and Optical Physics
- Atomic Physics
- Molecular Physics
- Radiometric Physics
- Quantum Metrology
- Ionizing Radiation
- Time and Frequency<sup>1</sup>
- Quantum Physics<sup>1</sup>

### **Manufacturing Engineering Laboratory**

- Precision Engineering
- Automated Production Technology
- Robot Systems
- Factory Automation
- Fabrication Technology

### **Materials Science and Engineering Laboratory**

- Intelligent Processing of Materials
- Ceramics
- Materials Reliability<sup>1</sup>
- Polymers
- Metallurgy
- Reactor Radiation

### **Building and Fire Research Laboratory**

- Structures
- Building Materials
- Building Environment
- Fire Science and Engineering
- Fire Measurement and Research

### **Computer Systems Laboratory**

- Information Systems Engineering
- Systems and Software Technology
- Computer Security
- Systems and Network Architecture
- Advanced Systems

### **Computing and Applied Mathematics Laboratory**

- Applied and Computational Mathematics<sup>2</sup>
- Statistical Engineering<sup>2</sup>
- Scientific Computing Environments<sup>2</sup>
- Computer Services<sup>2</sup>
- Computer Systems and Communications<sup>2</sup>
- Information Systems

---

<sup>1</sup>At Boulder, CO 80303.

<sup>2</sup>Some elements at Boulder, CO 80303.

QC  
100  
.45753  
#1295  
(173)

## ***NIST Technical Note 1295***

---

# ***Initial Graphics Exchange Specification Hybrid Microcircuit Application Protocol***

---

Curtis Parks  
Roger McCollough \*  
Charles Azu \*  
Larry Savage \*\*  
Patrick Toomey \*\*  
Thomas Makoski \*\*\*

Automated Electronics Manufacturing Programs  
National Institute of Standards and Technology  
Gaithersburg, MD 20899

January 1993

- \* Naval Command, Control & Ocean  
Surveillance Center, Research  
Development Test & Evaluation Division
- \*\* Raytheon Company
- \*\*\* International TechneGroup, Inc.



**U.S. Department of Commerce**  
Ronald H. Brown, Secretary

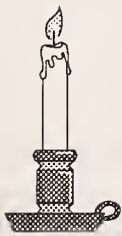
National Institute of Standards and Technology  
John W. Lyons, Director

---

National Institute of Standards  
and Technology  
Technical Note 1295  
Natl. Inst. Stand. Technol.  
Tech. Note 1295  
193 pages (Jan. 1993)  
CODEN: NTNOEF

U.S. Government Printing Office  
Washington: 1993

For sale by the Superintendent  
of Documents  
U.S. Government Printing Office  
Washington, DC 20402



**“Information is neither Matter nor Energy”**

*Norbert Wiener*

---

---

*Initial Graphics Exchange Specification (IGES)*

## **HYBRID MICROCIRCUIT APPLICATION PROTOCOL (AP)**

*Version 1.0: This document is the initial release of a complete application protocol for hybrid microcircuit technology. Included are refinements to prior preliminary versions, the missing Application Interpreted Model, comments from the hybrid design, manufacturing, and IGES communities. This version reflects the final work of the Navy Hybrid MicroCIM Team, together with the many people who have contributed technical material, participated in reviews, and comments.*

### **ABSTRACT**

An application protocol is an information systems engineering view of a specific product. The view represents an agreement on the generic activities needed to design and fabricate the product, the agreement on the information needed to support those activities, and the specific constructs of a product data standard for use in transferring some or all of the information required.

This applications protocol describes the data for hybrid microcircuits products in terms of a product description standard called the Initial Graphics Exchange Specification (IGES). More specifically, the Hybrid Microcircuit IGES Application Protocol (AP) specifies the mechanisms for defining and exchanging computer-models and their associated data for hybrid microcircuits in IGES format. The AP defines the appropriateness of the data items for describing the geometry of the various parts of a hybrid microcircuit (shape and location), the connectivity, and the processing and material characteristics.

## PREFACE

The Electricity Division of the Electronics and Electrical Engineering Laboratory and the Automated Manufacturing Research Facility of the Center for Manufacturing Engineering at the National Institute of Standards and Technology (NIST) have completed a program entitled “A Data Format Specification for Hybrid Microcircuit Assemblies.” This project was sponsored by the Office of the Assistant Secretary of the Navy for Manufacturing Technology and was managed by the Naval Command, Control & Ocean Surveillance Center, Research Development Test & Evaluation Division (NCCOSC, RDT&E), San Diego, Contract No. N0001991IPAKC1R, MOD/AMEND No. 0A-001. The project objective was the development of a specification for a neutral format to promote the exchange of design and manufacturing data for hybrid microcircuit products.

The ultimate scope of this AP will include the various aspects of hybrid microcircuits including the specification control drawings, circuitry and parts layout, and information concerning their fabrication. The specified hybrid microcircuit model is sufficiently detailed to support the design release, fabrication, and final assembly of a hybrid system.

IGES is designed to support a broad range of applications and information, and it is recognized that few implementations will support all of the specification. An application protocol defines a logical subschema of the IGES specification, the usage of the subschema, and the necessary benchmarks for testing implementations. The application protocol for hybrid devices builds on the previous work of the Electrical Applications Committee of the IGES/PDES Organization. Such documents are seen as important for the development of STEP (Standard for the Exchange of Product Model Data) application protocols.

The title denotes the general class of the product, including hybrid microcircuit assemblies (HMA) and multichip modules (MCM). The data structures defined in this document are proposed for testing by representatives of the hybrid microcircuits industry, members of the Navy’s MicroCIM Program, and the IGES/PDES Electrical Applications Committee in order to meet a broad user community of hybrid microcircuits applications. This AP will be tested and refined in developing a revision to MIL-D-28000A<sup>1</sup> Class 3. This revision will define a new MID-D-28000 class for the transfer of hybrid microcircuit data by use of future versions of IGES.

The members of the program team also note that other data formats may be employed. They would encourage continuation of work to achieve an industry consensus of the activity and reference model sections (Appendix A and 3.2 respectively) and additional interpretation (sec. 5) models as needed for each additional format supported. Comments on this document should be sent to:

Curtis Parks  
Automated Electronics Manufacturing Programs  
National Institute of Standards and Technology  
Building 220 Room B-344  
Gaithersburg, MD 20899  
(301) 975-3517 (Parks)  
E-Mail: parks@eeel.nist.gov

---

<sup>1</sup>. MIL-D-28000 is the Department of Defense specification that identifies the requirements to be met when product definition data is delivered in IGES format.

The following computer system developers have participated in the development of this AP, and may be contacted regarding translator preparation information:

**Intergraph-Dazix**

One Madison Industrial Park  
Huntsville, AL 35894  
(205) 730-2000  
Anthony Prince

**Scicards**

7796 Victor Mendon Road  
Fishers, NY 14453  
(716) 924-9303  
Diane Elmer

**Mentor Graphics**

1001 Ridder Park Drive  
San Jose, CA 95131  
(408) 451-5639  
Dave Kehmeier

**Cadence Design Systems, Inc.**

Two Omni Way  
Chelmsford, MA 01824  
(508) 256-2300  
Randy Lawson

**Prime-ComputerVision**

100 Crosby Drive  
Bedford, MA 01730  
(617) 275-1800  
Bernard Gilbert

**Future Directions**

The Application Activity Model (Appendix A) and Application's Information Model (sec. 4.2) contain sufficient detail to support design release, fabrication, and final assembly of hybrid system. The IGES models (sec. 5) in this document, however, are not meant to fully support hybrid microcircuit product testing, analysis, and manufacturing. A full life-cycle data standard—possibly based on the Standard for the Exchange of Product Model Data (STEP)—will be necessary to support all phases of hybrid microcircuit processing.

This document does not complete the fabrication definition in terms of the sequence of processing steps and the parameters used in those steps. These steps and parameters are expected to be published by NIST in a separate document. Review and comments on this related document are welcome as well. A copy of the draft of the hybrid processing steps and parameters may be obtained from the address given at the end of the Preface section.

The scope of this AP AIM is currently limited to layered electronic product (LEP) information contained in electronic computer-aided design (ECAD) systems. These systems are in wide-spread use. Their ability to translate data between dissimilar systems is a high priority in the user community. IGES serves as the implementation for this information because most ECAD suppliers are familiar with the specification and support it in their software packages.

A broadened scope for this AP that includes manufacturing, test, simulation, behavior, and documentation is desired by users and manufacturers of hybrids. Much of this information is outside the scope of most ECAD systems and the IGES specification.

**About the Document**

The style, format, and much of the material for this application protocol was taken from the “3D

Piping IGES Application Protocol.” That AP specifies the mechanisms for defining and exchanging 3D piping system models in IGES format.<sup>2</sup> The “3D Piping IGES Application Protocol” was the first IGES AP to be delivered to industry and led to the development of STEP (Standard for the Exchange of Product Model Data) application protocols. The authors of this document are indebted to Mark Palmer for his work and the guidance that it provides. It is the authors’ belief that if the CAD/CAM industry is to use application protocols consistently, we need consistent application protocols.

Preparation of this document is a tribute to the ability to move text and graphics between applications and computer systems.<sup>3</sup> The text was originated in WordPerfect™ DOS™ and filtered into FrameMaker™ 2.1 on a Sun™ workstation for the original formatting and some of the graphics. The AAM model was developed in Design/IDEF™, and glossary in Hypercard; both on the Macintosh™. The ARM was drawn in MacDraw II™. The AIM was developed at International TechnoGroup Inc. (ITI) where the text was written in Word™ for DOS and the graphics drawn in AutoCAD™. The graphics were transmitted to Raytheon in IGES format where they were edited and translated into FrameMaker™ MIF format. Final document assembly was done in FrameMaker™ 3.0/Mac and LASER-printed from Frame’s PostScript™ output.

## ACKNOWLEDGMENTS

The authors thank the following individuals for contributions to the development of this document:

Thomas Leedy—the author of the first work toward this document—and Robert Palm, NIST; Mike Bare and David Weins, Intergraph, Inc.; John Buckley, Raytheon, Inc.; Kim Cannon, Kulicke and Soffa Industries, Inc.; Terry Sampite, NCCOSC; Dave Mattei, ITI, Inc.; Larry O’Connell (Chairman of the Electrical Applications Committee, IGES/PDES Organization), Sandia Laboratories; Robert Unger, Computer Sciences Corporation; Charlie Jordan, Dean Marshall, and Don Slutz, CTS Inc.; and many others to be included in future revisions ....

---

<sup>2</sup> Palmer, M. E. and Reed, K. A., “3D Piping IGES Application Protocol, Version 1.0” NISTIR 4420, Available from the National Technical Information Service (NTIS), Springfield, VA 22161, October 1990, (257 pages).

<sup>3</sup> Wordperfect and DOS are trademarked by Microsoft Corp.; Framemaker is trademarked by Frame Technology Corp.; Sun is trademarked by Sun Microsystems, Inc.; Design/IDEF is trademarked by Meta Software Corp.; Hypercard and Macintosh are trademarked by Apple Computer, Inc.; AutoCAD is trademarked by Autodesk, Inc.; and PostScript is trademarked by Adobe Systems, Inc. Trademarked products were mentioned in this document as examples of the range of possible products and are not necessarily endorsed by NIST.

---

# *Table of Contents*

---

---

Abstract	iii
Preface	iv
Future Directions	v
About the Document	v
Acknowledgements	vi

## 1. INTRODUCTION 1

---

1.1. Purpose	1
1.2. Background	1
1.2.1. Hybrid Complexity	2
1.2.2. Consistent Information for Concurrent Engineering	2
1.3. APPLICATION PROTOCOL CONTENTS	3

## 2. NORMATIVE REFERENCES 3

---

## 3. DEFINITIONS 5

---

3.1. IGES Application Protocol Definitions	5
3.2. Hybrid Application Definitions	7

---

## 4. INFORMATION REQUIREMENTS AND APPLICATION REFERENCE MODEL 23

---

- 4.1. Units of Functionality (UoF) 23
  - 4.1.1. Unit of Functionality Definitions 24
  - 4.1.2. UoF and ARM Correspondence 24
- 4.2. Application Reference Model 25
  - 4.2.1. Descriptions of the ARM Data Constructs 25
    - 4.2.1.1. ARM Methods and Language 25
  - 4.2.2. Data Construct Definitions 27
    - 4.2.2.2. Data Construct Assertions 27
  - 4.2.3. ARM Diagrams 28

## 5. IGES APPLICATION INTERPRETED MODEL 35

---

- 5.1. ARM to AIM Mapping 36
- 5.2. IGES Structure and Syntax of the Application Interpreted Model 36
  - 5.2.1. IGES File Structure 36
  - 5.2.2. Global Values and Entities List 37
  - 5.2.3. Basic Syntax used in the AIM 39
    - 5.2.3.1. Object Definition Block 39
    - 5.2.3.2. Object Instance Block 40
    - 5.2.3.3. Object Value Block 41
    - 5.2.3.4. Object Reference Mechanism 42
  - 5.3. AIM Object Models 43
    - 5.3.1. Interface Object Models 43
      - 5.3.1.1. LEP Part Library IGES File 43
      - 5.3.1.2. LEP Physical Layout IGES File 44
      - 5.3.1.3. LEP Technical Illustration IGES File 45
    - 5.3.2. LEP-Specific Object Models 46
      - 5.3.2.1. Alternate Component Associativity 46
      - 5.3.2.2. Component Placement Associativity 47
      - 5.3.2.3. Part Placement Boundary 48
      - 5.3.2.4. Component Placement Keepin 49
      - 5.3.2.5. Component Placement Keepout 50
      - 5.3.2.6. Part Thermal Outline 51
      - 5.3.2.7. Crossover 52
      - 5.3.2.8. Decoupling Capacitor Associativity 53
      - 5.3.2.9. Drawing Definition 54
      - 5.3.2.10. Drawing Instance 55
      - 5.3.2.11. Electronic Component Definition 56
      - 5.3.2.12. Electronic Function Definition 57
      - 5.3.2.13. Fiducial Associativity 58
      - 5.3.2.14. Fiducial Definition 59
      - 5.3.2.15. Fiducial Instance 60
      - 5.3.2.16. Generic Part Definition 61
      - 5.3.2.17. Generic Part Instance 62
      - 5.3.2.18. Hole 63
      - 5.3.2.19. Join 64
      - 5.3.2.20. Jumper Wire 65
      - 5.3.2.21. Keepin/Keepout 66
      - 5.3.2.22. Land 67

---

## Contents

---

5.3.2.23. Laser Trim Path	68
5.3.2.24. Layer Outline	69
5.3.2.25. LEP Artwork Stackup Property	70
5.3.2.26. LEP Part Placement Boundary Property	71
5.3.2.27. LEP Definition	72
5.3.2.28. LEP Fixed Component Placement Property	74
5.3.2.29. LEP Instance	75
5.3.2.30. LEP Object Type/Sub-Type	76
5.3.2.31. LEP Physical Layer Description	77
5.3.2.32. LEP Substrate Hole Property	78
5.3.2.33. Level to LEP Map	79
5.3.2.34. Machined Hole	80
5.3.2.35. Machined Hole Figure Associativity	81
5.3.2.36. Machined Hole Figure Definition	82
5.3.2.37. Machined Hole Figure Instance	83
5.3.2.38. Net	84
5.3.2.39. Net Connection Associativity	86
5.3.2.40. Package Symbol Definition	87
5.3.2.41. Package Symbol Instance	89
5.3.2.42. Padstack Definition	91
5.3.2.43. Padstack Instance	92
5.3.2.44. Panel Definition	93
5.3.2.45. Panel Instance	94
5.3.2.46. Pin	95
5.3.2.47. Pin Out Associativity	97
5.3.2.48. Routing Keepin	98
5.3.2.49. Routing Keepout	99
5.3.2.50. Test Point	100
5.3.2.51. Test Point Associativity	101
5.3.2.52. Trace Keepout	102
5.3.2.53. Variable Test	103
5.3.2.54. Via	104
5.3.2.55. Via Keepout	105
5.3.2.56. Wire Bond	106
5.3.3. Display Geometry Object Models	107
5.3.3.1. Arc	107
5.3.3.2. Circle	108
5.3.3.3. Closed Curve	109
5.3.3.4. Composite Curve	110
5.3.3.5. Curve	111
5.3.3.6. Display Geometry	112
5.3.3.7. Ellipse	113
5.3.3.8. Elliptical Arc	114
5.3.3.9. Geometry Figure Definition	115
5.3.3.10. Geometry Figure Instance	116
5.3.3.11. Hyperbolic Arc	117
5.3.3.12. Line	118
5.3.3.13. Modified Geometry Figure Instance	119
5.3.3.14. Multi-Line	120
5.3.3.15. Non-Closed Curve	121
5.3.3.16. Parabolic Arc	122
5.3.3.17. Parametric Spline Curve	123
5.3.3.18. Planar Composite Area	124
5.3.3.19. Polygon	125
5.3.3.20. Point	126
5.3.3.21. Predefined Planar Shape	127
5.3.3.22. Rational B-Spline Curve	128
5.3.3.23. Simple Geometry Figure Instance	129
5.3.3.24. Text String	130

---

## Contents

---

5.3.4. Miscellaneous Object Models	131
5.3.4.1. Attribute Table Definition	131
5.3.4.2. Attribute Table Instance	132
5.3.4.3. Definition Extents	133
5.3.4.4. Generic Data Property	134
5.3.4.5. Hierarchy Property	135
5.3.4.6. Instance Level Display Property	136
5.3.4.7. Modified Entities Definition	137
5.3.4.8. Modified Network Subfigure Instance	138
5.3.4.9. Modified Subfigure Instance	139
5.3.4.10. Name	140
5.3.4.11. Network Subfigure Definition	141
5.3.4.12. Network Subfigure Instance	142
5.3.4.13. Object Locator	143
5.3.4.14. Part Number Property	144
5.3.4.15. Region Restriction	145
5.3.4.16. Subfigure Definition	146
5.3.4.17. Subfigure Instance	147
5.3.4.18. Text Display Template	148
5.3.5. DE Referenced Object Models	149
5.3.5.1. Color Definition	149
5.3.5.2. Level Definition	150
5.3.5.3. Line Width Definition	151
5.3.5.4. Region Fill Definition	152
5.3.5.5. Transformation Matrix	153
5.3.5.6. Transformation (Mirrored)	154
5.3.5.7. Transformation Matrix (Standard)	155
5.3.6. DE Section Object Models	156
5.3.6.1. Associativity DE	156
5.3.6.2. Color Definition DE	157
5.3.6.3. Definition DE	158
5.3.6.4. Geometry DE	159
5.3.6.5. Instance DE	160
5.3.6.6. Property DE	161
5.3.6.7. Transformation Matrix DE	162

## 6. Implementation and Conformance Testing Guidelines 163

---

6.1. PROCESSOR CONFORMANCE REQUIREMENTS	163
6.2. Test Purposes	164
6.3. Enumerated Application Protocol Test Groups	165

## A. ACTIVITY MODEL CONTENTS A 167

---

## B. Technical Discussions 187

---

---

# *Table of Figures & Diagrams*

---

---

## 4. ARM Figures

---

4-1. Component Parts of an IDEF Relationship 26

4-2. Cardinality 26

4-3. The Categorization Structure 27

---

## 4. ARM Diagrams

---

View 4-1 Top-Level Entities 29

View 4-2 Expanded Dependents of Pattern 30

View 4-3 Expanded Dependents of Hybrid Version 31

View 4-4 Expanded Dependents of Hybrid Assembly Occurrence 32

View 4-5 Expanded Component Model 33

View 4-6 Expanded Dependents of Assembly Consumables and Deposition  
Component 34

---

## 5. AIM Figures

---

5-1. IGES Object and Referencing 40

5-2. References to Previously Defined Object 41

5-3. Object Field Value Restrictions 41

5-4. Reference Mechanism 42

5-5. Representation Mechanism 42

---

## 5. AIM Object Models are listed in the Table of Contents

---



# Initial Graphics Exchange Specification (IGES) HYBRID MICROCIRCUIT ASSEMBLY APPLICATION PROTOCOL

## 1. INTRODUCTION

### 1.1. Purpose

This application protocol (AP) for hybrid microcircuit assemblies uses the Initial Graphics Exchange Specification (IGES) for the representation of the product definition and for the exchange of these definitions from one hybrid microcircuit defining application to another. Since the hybrid microcircuit application protocol makes use of a specific interpretation of entities in the IGES file, both the sending and receiving sites must support this entire hybrid microcircuit application protocol, not just the IGES entities listed.

### 1.2. Background <sup>4</sup>

Hybrids are defined to be modules or subcircuits that are incorporated into larger electronic assemblies, such as printed circuit boards. Typically, a hybrid is connected to the larger assembly with external leads or pins. A hybrid incorporates an insulating substrate onto which a mix of integrated circuits and other electronic components (such as thick- and thin-film devices) are interconnected.

A neutral data format serves several purposes: It permits the interchange of data between computer-aided design (CAD) and computer-aided manufacturing (CAM) systems. It allows the archiving of the hybrid design in a format that can be used in the future, even if the original CAD or CAM systems or their software are no longer in use.

There are a number of motivations for developing a specified representation for hybrids. The most compelling motive is to reduce the errors created by different interpretations of a format as used for a particular product. A specified representation for hybrids can also minimize cost and maximize efficiency in the design and maintenance of translators. These uniform applications can provide means for coping with the increasing complexity of hybrids. In current practice, there is often the need for manual intervention in order to transfer the data between the CAD workstations and to the CAM stations that produce the hybrid. Even in automated systems, the problem is compounded by the fact that a data "translator" must be written for each pair of machines that must exchange data. If there are  $n$  machines in the system—*potentially*  $n(n-1)$ —translators are needed.

### Data hub concept

A neutral format serves as a data "hub." Each station served must only translate data from its own

---

<sup>4</sup> Harrison, Randy J. and Palmer, Mark E., "Guidelines for the Specification and Validation of IGES Application Protocols" NISTIR 88-3646, January 1989. (Available from the National Technical Information Service (NTIS), Springfield, VA 22161), October 1990, (110 pages).

format to the neutral format of the hub to be able to interchange with any other station interfacing with the hub. For example, data could be exported from a CAD workstation to the hub and be available there in neutral format for extraction by other CAD workstations and CAM machines. In this arrangement, for  $n$  machines in the system, there are *potentially*  $2n$  translators needed, a substantial reduction.

### 1.2.1. Hybrid Complexity

Hybrid microcircuits have become increasingly complex in nature. One measure of this increased complexity is the ratio of the area of active elements (usually silicon chips) to the unoccupied area of the substrate. In a single-chip package of a monolithic integrated circuit, the ratio is about 1:20; in today's typical hybrid, the ratio is from 1:10 to 1:6. Present engineering efforts have the goal of raising this ratio to 1:1, i.e., 50% of the substrate would be covered by silicon chips. These high-density hybrids are often referred to as multichip modules, or MCMs. To cope with this expanding complexity, hybrid manufacturing will increasingly depend on CAD and CAM techniques. For practical implementation of combined CAD and CAM techniques, it is important to have a single electronic representation of the CAD data available for interfacing with CAM environments. The representations described in this AP apply to both MCM and conventional hybrid technology.

Many hybrid manufacturers still use extensive paper documentation, such as prints and drawings, to document their product during manufacturing. Often, these drawings are produced on CAD stations that contain information that is not represented on the drawing and yet may be useful during the design process. As automated manufacturing methods become more available, such "paper" documentation will impede manufacturing. Further, as the complexity of hybrids increases, it will become much more necessary to convey this information to manufacturing machines in computer-comprehensible form.

### 1.2.2. Consistent Information for Concurrent Engineering

Another benefit from a unified representation of the data describing an hybrid is the ability to achieve concurrent engineering, which in the case of an hybrid permits various automated and human resources to be applied to the design of the hybrid simultaneously. Since these resources share common data regarding the design, it is possible for various groups of engineers to refine the mechanical, electrical, thermal, and testability characteristics of the hybrid in a much shorter time than would be required otherwise. In addition, concurrent engineering permits different application specialists to work in parallel with the designer. Thus, for example, those that are responsible for the manufacturing, assembly, quality, and reliability of an hybrid design are able to provide suggestions concerning the design from its inception.

This method of business is in sharp contrast to the traditional methods where each department contributed sequentially to the design process of an hybrid. Concurrent engineering methods promote a combined effort where all information builds on an existing model and changes can be easily accommodated through the separate functional areas. Since changes in the design are incorporated early in the design cycle, the costs of such changes is decreased. The result of effective concurrent engineering is a product at lower cost and with a shorter design cycle than would be realizable with traditional methods. Increased product quality results from accurate data transfer, as opposed to manual regeneration of CAD data on succeeding systems.

There are several existing neutral file specifications to describe electrical and electronic functions.

These include specifications developed by the Institute for Interconnecting and Packaging Electronic Circuits (IPC), the Electronic Design Interchange Format (EDIF), the Initial Graphics Exchange Specifications (IGES), and the VHSIC Hardware Description Language (VHDL). These neutral file specifications may support many of the data elements needed to represent an hybrid design. Adding these formats is encouraged, and may be accomplished by adding the appropriate models to section 5 of this AP. During such additions, the remaining sections should be refined by agreement between the organizations that are responsible for the formats. Conflicting information requirements (e.g., sections 3 and 4 of this document) among different formats are not considered appropriate to the goals of product data consistency.

### 1.3. APPLICATION PROTOCOL CONTENTS

Section 2 of the AP provides a list of documents which are used in the construction of this protocol. Definitions of terms used in the AP are listed in alphabetical order in section 3. Part 3.1 of this section lists terms contained in the text of the AP while part 3.2 are terms contained in the various models (AAM, ARM, AIM) of the AP. Terms in both sections are listed along with reference to the models in which they appear.

The Application Reference Model (ARM) is explained and presented in section 4. The ARM is constructed in terms used within the electronic design and fabrication community (i.e., an external schema). For example Part and Component are used, and are given definitions appropriate to those found in engineering as related to the use of CAD systems and supporting libraries. The concept of units of functionality as they apply to the ARM is described. The IDEF1X modeling technique is used to develop the ARM and a brief tutorial on how to read the model is included.

The Application Interpretive Model (AIM) is described and presented in section 5. The mapping of the ARM to AIM is explained. The objects declared in this section are associated to general and specific CAD data items (i.e., an internal schema). A description of the IGES file structure and the breakdown of its sections is given. A modeling syntax is used to develop the AIM and a brief tutorial on how to read the model is included.

Section 6 details implementation and conformance guidelines for this Application Protocol. Process conformance requirements and testing purposes are given. Appendix A contains the Activity Model which puts the AP into scope. Appendix B has a parameter listing of typical hybrid microcircuit processing parameters/variables and their values.

### 2. NORMATIVE REFERENCES

The following documents constitute a normative part of this document:

IPC-T-50E, "Terms and Definitions for Interconnecting and Packaging Electronic Circuits," February, 1991, Institute for Interconnecting and Packaging Electronic Circuits, Lincolnwood, IL 60646.

MIL-H-38534, "Hybrid Microcircuits, General Specification for," 31 March 1989.

Reed, Kent; ed, The Initial Graphics Exchange Specification (IGES) Version 5.1, September, 1991, National Computer Graphics Association, Fairfax, VA 22031.



### 3. DEFINITIONS

#### 3.1. IGES Application Protocol Definitions

**Application:** An enterprise process that puts product data to use. The scope of an application is defined by the class of product, the supported stages in the life cycle of the product, the uses of the product data, and the disciplines that participate in that use.

**Application Activity Model (AAM)** - A structured decomposition of the tasks which are followed to achieve the particular product defined by the AP. The AAM identifies the scope of the AP as well as the activities which create and use the information being defined. The AAM is constructed to be generally representative of the industry, and includes processes which are, or could be, largely automated.

**Application Interpreted Model (AIM)** - An information model that identifies the information structures of a particular data format specification. The AIM is defined to accomplish a physical implementation of an associated application reference model (ARM). This AIM is prepared at a level of abstraction that is sufficient for selecting the necessary entities for an application.

**Application Protocol (AP):** Defines the scope and information domain of an application and specifies the rules for using IGES, or some other standard, to enable unambiguous transfer of the application information, and the testing of those transfer implementations.

**Application Reference Model (ARM)** - An information model that describes the information structures and constraints for an application area. The ARM is defined in terms of Entities, Attributes, and Relationships. The information model uses application specific terminology and rules familiar to an expert from the application area. The model is independent of any physical implementation and can be validated by an expert from the application area.

**Application Subset** - An unambiguous set of entities which span the data requirements of the specified application. The set of entities is determined on the basis of the Application Reference Model.

**Assembly** - In general (e.g., from Websters): Parts fitted together to make a whole. The assembly referred to in this AP is taken to mean parts placed on, and/or connected to, an interconnecting part generally in the form of a flat substrate on which has been deposited alternate layers of metalized patterns and insulation material; the whole of which has been defined as to provide a specified part of the function of a system. An assembly may be used as a part on another assembly.

**Attribute** - A property or element of information associated with an Entity. An instance of the attribute must exist for any instance of the Entity to which it belongs.

**Entity** - The basic unit of data classes in the ARM. Also the basic data types identified in the AIM. The term applies to single units which may be individual elements of geometry, individual elements of annotation, or collections of geometry or annotation elements that are combined to form more complex data structures.

**IGES Postprocessor** - A software unit that transfers CAD information from the IGES format to the CAD database format of a particular system. The software is usually developed and maintained by a commercial CAD system vendor.

**IGES Preprocessor** - A software unit that translates CAD information from the CAD database format of a particular CAD system to the IGES format. The software unit is usually developed

and maintained by a commercial CAD system vendor.

**Information Configuration Control** - An approach that consists of specifying, documenting, and controlling both the creation and modification of information and the subsequent translation and exchange of the information between different systems and formats. The approach requires substantial documentation for both the syntax (the format) and the semantics (the meaning) attached to an item of information.

**Instance** - In general (e.g., from Websters): A detail or circumstance. In this AP an instance indicates that a specific member of an object class is being referenced. An example of an object class may be the assembly as identified by a drawing number. An example of an instance may be a completed assembly identified by a serial number.

**Layered Electrical Product (LEP)** - A broad category of electronic product types which are characterized by a two or more laminar strata stacked in sequential order. The completed structure serves to conduct electrical signals and may contain passive or active electrical functional elements. The structure is usually designed using two-dimension (2-D) graphics which result in photo-process tooling. Additional components or other LEPs may be added to complete the assembly. Descriptions within this document which apply additionally to products such as integrated circuits, printed circuit boards, flex harnesses are labeled with this term.

**Occurrence** - In general (e.g., from Websters): Anything that happens or takes place. In this AP the term is sometimes used to label an object class which exists as a result of a sepcific grouping of two or more other object classes.

**Product** - A result produced by specified activities or used for specified activities.

**Product Data** - The set of data elements that is necessary to fully support a product over its expected life cycle. The set of data elements includes all of the product definition data plus other data pertaining to the operation and maintenance of the product until it is removed from service.

**Product Definition Data** - The set of data elements that completely define a product for a certain discipline; a subset of product data. This set of data elements includes the geometry, topology, features, tolerances, and relationships necessary to completely define a component product or an assembly of products and is structured such that it can be used by one or more applications.

**Relationship** - The identified association of two entities to each other. The two entities and their relationship taken together constitute a natural language *role* expressed in the data model.

Example: Assuming the entities "Car" and "Person" are associated with relationship "Owned" in a data model Then the role may be expressed in natural language as: "A Car is owned by a person." The exact role stated depends on the modeling language's interpretation specifications.

**Semantics** - The meaning that is given or assigned to an item of information. The meaning is assigned to an item of information on the basis of its application area.

**Syntax** - The structure of expressions in a language. [3] This structure is described in a specification such as IGES.

**Unit of Functionality** - A collection of entities, attributes and relationships that conveys one or more well-defined concepts (within the scope of the AP) such that removal of any component would render the concept(s) incomplete or ambiguous. (See "Current Issues on STEP APs," 10/9/91.)

### 3.2. Hybrid Application Definitions

The bracketed character following the term indicates that the definition applies primarily to the AAM [A], AIM [I], or the ARM [R].

Note: definitions preceded by (T50) are from IPC-T-50E, December 1991.

**ANNOTATION** - [R] Text or legend pertinent to a design; text may appear as data related to legend on a multilayer substrate, lettering on a drawing, or other types of symbols.

**APERTURE CODE** - [R] Code representing aperture number used in plot file intended for a plotter such as a Gerber Plotter.

**APERTURE NUMBER** - The number for a photoplotter aperture setting, number used in pin and pad tables, and formatter table corresponding to a position on the aperture wheel.

**APERTURE SHAPE** - [R] Shape of aperture, such as one of the following: round, square, donut.

**APERTURE SIZE** - [R] The x,y dimensions of the aperture such as width or diameter where appropriate.

**ART WORK (T50)** - [R] An accurately-scaled configuration that is used to produce the artwork master used for production.

**ART WORK GEOMETRY (target) (outside circuit)** - [R] A collection of primitive shapes such as arcs, areas, and lines.

**ART WORK TEXT** - [R] Identifying text which calls out the hybrid product number and configuration number as well as program configuration for the hybrid art work. It identifies layer, revision, hybrid number.

**ASPECT RATIO (of Deposition Resistor)** - [R] The ratio of the length of a thick or thin film resistor to its width, or the ratio between the resistance of the resistor and the sheet resistivity of the ink. This is also the number of effective "squares" in the design of a resistor.

**ASSEMBLY CONSUMABLES** - [R] A type of consumable that becomes part of the finished product. See also Consumable.

**ASSEMBLY ID** - [R] All information needed to uniquely identify a particular assembly, manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, case style, and other product notation.

**ASSEMBLY OCCURRENCE** - [R] Either a single product which is defined to become part of an assembly, or two products which are identified as items to be assembled into the next higher assembly. The occurrence identified may be noted in a bill of materials, or may be in-process work which must be identified for manufacturing tracking.

**ASSEMBLY OCCURRENCE ID** - [R] All information required to uniquely identify (ID) a product and the assembly it is assembled to. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, case style, and other product notation.

**ASSEMBLY TYPE** - [R] The name of the class of assembly which indicated the general stage of completion of the electronic product. Examples are screened substrate, subassembly, component assembly, and final assembly.

**ATTACHMENT** - [R] Method used to describe how a component can be held on to the substrate such as solder, or epoxy.

**ATTACH MATERIAL PATTERN** - [R] Pattern associated with a component for the purpose of specifying the location and shape of an attachment medium or material.

**BACK PAD POLARIZATION** - [R] Description of which pin is electrically connected to the back pad of a component such as a diode or IC chip.

**BACK PAD POLARIZATION NAME** - [R] Name associated with the back pad such as anode.

**BILL OF MATERIALS** - [R] A formatted list of products (instances of Hybrid Assembly Components) used for a particular assembly.

**BLIND VIA** - A via that is visible from only one side or the other of a design. (Derived from Via attributes.)

**BONDING PADS** - [R] Areas of metallization on the component and the hybrid substrate that permits connection of the wire or circuit elements.

**BURIED VIA** - A via hole not extending to the surface. A buried via is completely contained within the inner layers of a design and therefore is not visible from the outside layers. May be referred to as an interstitial via hole. (Derived from Via attributes.)

**CAD LAYER** - [R] A method of separating information in a CAD system for the purpose of display or processing. Some CAD layers correspond to artwork layers.

**CAGE NUMBER** - [R] The military-assigned identification of the manufacturer responsible for the product definition.

**CAPACITOR COMPONENT** - [R] A kind of component used to add capacitance to a hybrid circuit.

**CAPACITOR MATERIAL** - [R] The type-name for a capacitor derived from the dielectric material of the capacitor

**CATCH PAD** - [R] Metallization patterns on a conductive layer associated with a via which aid in the interconnection of a via with its associated traces.

**CHECKPLOT SCALE (T50)** - [R] Drawing scale used on interim drawing for graphical data verification. (called a check plot.)

**COMPONENT ATTACH** - [A] The placing of a component (chip) on a substrate or header in a manner which causes it to mechanically bond.

**COMPONENT LOCATION PLACEMENT TOLERANCE** - [R] The amount of displacement from the specified location which is acceptable.

**COMPONENT LOCATION X Y** - [R] The coordinates specified for the location of a component within an assembly.

**COMPONENT ORIENTATION (T50)** - [R] The direction in which the components on a printed board or other assembly are lined up electrically with respect to the polarity of polarized components, with respect to one another, and with respect to the board outline.

**COMPONENT PLACEMENT RESTRICTION** - [R] An area on substrate where components can not be placed.

not be placed.

COMPONENT POSITION - [R] The location at which a component is placed.

COMPONENT SELECTION - [R] A set one or more alternate chips to be specified in the design of a hybrid, one of which is selected at the time of manufacture of a particular hybrid.

COMPONENT TOLERANCE - [R] The range of acceptable component values; usually specified as a percentage of the nominal specified value.

COMPONENT VALUE - [R] The parameter associated with some component types which may be used in the fabrication of the components.

COMPONENT VALUE TOLERANCE - [R] A range of permissible product's values.

COMPONENT VOLTAGE RATING - [R] Maximum voltage specified that can be placed across a component.

CONDUCTIVE PATTERN - [R] The configuration or design of the conductive material on the substrate. For a hybrid, the pattern includes conductors, lands, and through connections (vias) when these connections are an integral part of the manufacturing process.

CONDUCTIVITY, ELECTRICAL - [R] The capability of a material to carry an electrical current. The reciprocal of resistivity.

CONSUMABLE - [R] An in-process or an end item material supplied in bulk form.

CONSUMABLE ID - [R] All information needed to uniquely identify a particular consumable, manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, and other material notation.

CONSUMABLE NAME - [R] The name given to bulk-purchase materials used in the assembly process, such as solder, flux, etc.

CONSUMABLE PROPERTY - [R] Properties of a consumable such as shelf life, expiration date.

CONSUMABLE PROPERTY NAME - [R] The name of a Consumable Property.

CONSUMABLE PROPERTY VALUE - [R] The measurement value associated with a Consumable Property.

CONSUMABLE TYPE - [R] The generic classification given to consumables, such as epoxy.

CROSSOVER - The transverse crossing of metallization paths without mutual electrical contact achieved by the deposition of an insulating layer between the conducting paths at the area of crossing. Dielectrics can be used with crossover conductive patterns, acting as a bridge over previously screened conductive material. (derived from trace geometry.)

DEFAULT DESIGN RULE - [R] The specifications which are followed during layout of the patterns on the layers of an electronic assembly. Examples are the maximum trace width, or the minimum conductor spacing.

DEFAULT DESIGN RULE DESCRIPTION - [R] The description of a Design Rule that is employed when no other rule is specified.

DEFAULT DESIGN RULE NAME - [R] The name associated with a Design Rule.

DEPOSITION COMPONENT - [R] Components which are fabricated coincidentally with the

interconnects as opposed to components which are attached to the substrate after the interconnect network is complete.

**DEPOSITION RESISTOR** - [R] The deposition of resistor material which is formed as part of the conductive circuitry on a substrate layer. The resistor is a component in the sense of the electrical function of the circuit, but not in the sense of a separate product to be assembled to the completed substrate.

**DEPOSITION SEQUENCE NUMBER** - [R] A particular layer's position on the hybrid substrate with respect to the first layer.

**DEPOSITION TYPE** - [R] A category used to describe the technology used (THICK or THIN film) to create the component.

**DERATING** - [R] A factor which is applied to a product parameter to insure that reliability requirements are met; such as derate resistor power rating by 50%.

**DESIGN RULE** - [R] A guideline that determines behavior with respect to specified design parameters. Becomes a constraint on the functional and physical layout. An example is a rule that ensures that minimum distance between elements in a design file is maintained.

**DESIGN RULE CHECK (DRC)** - [R] A process to enforce the design rules.

**DESIGN RULE VALUE** - [R] The measurement assigned to a particular restriction for a product's design.

**DEVICE PIN ASSOCIATIVITY** - [R] Functional relationships among pins that are needed to allow operations such as gate swapping or pin swapping to improve trace routing

**DIE** - [A] The uncased and normally leadless form of an electronic component that is either active or passive, discrete active device or integrated circuit.

**DIE BONDING** - [A] The attachment of an integrated circuit chip to a substrate or header.

**DIELECTRIC** - [R] An insulating material used to separate conductors.

**DIELECTRIC CONSTANT** - The ratio of the capacitance,  $C_x$ , of a given configuration of electrodes with a specified dielectric, to the capacitance  $C_v$ , of the same electrode configuration having a vacuum as a dielectric.

**DIELECTRIC LOSS ANGLE** - [R] The difference between 90 degrees and the dielectric phase angle given a set of operating conditions. May be referred to as the dielectric phase difference.

**DIELECTRIC OUTLINE** - [R] The boundary of an insulating layer.

**DIELECTRIC STRENGTH** - The maximum voltage that a dielectric can withstand, under specified conditions, without resulting in a voltage breakdown. Usually expressed as volts per unit length.

**DISSIPATION** - [R] The tendency for fluids or energy to distribute evenly within a medium. This tendency is usually associated with the ability of a material shape to remove heat or power from physical devices and circuits.

**DISSIPATION FACTOR** - [R] A measure of insulating or dielectric materials to absorb some of the energy in an alternating current signal.

**DOCUMENTATION TEXT** - [R] Words (strings) which exists on documentation.

operation.

**EQUIPMENT** - [R] The identification name of machine types that are used as the means to complete a process step during manufacture of a device. Examples are a pick-and-place machine or a solder-joint inspection machine.

**ELECTRONIC PACKAGE** - [R] (See Package.)

**FILE ID** - [R] The unique identification of a data file stored in or intended for a computer system. For files containing product information, the identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, and other product notation.

**FILM** - (See Thick Film or Thin Film.)

**FILM MATERIAL** - [R] Material used in thin and thick film processes to fabricate components and circuitry.

**FUNCTION TYPE** - [R] The category describing the use of a particular artwork geometry such as Pad, Registration Mark, Conductor, Dielectric Edge, Text.

**GENERIC NAME** - [R] A commonly accepted product identification, such as 54LS04 or 2N2222.

**GEOMETRY** - [R] The constructs which are used to describe shapes of objects to be presented, or to which a product is to be fabricated. The description is usually in terms of a set of spatial coordinates and the identification of the curve-type to be constructed from the coordinates.

**GEOMETRY ELEMENT** - [R] A feature used to identify the meaning of, or use for, a collection of geometries. Examples from assemblies are countersink, keyway or threads. Examples from electrical planar designs are line, circle, area, etc.

**GEOMETRY LINE WIDTH** - [R] A measurement of the distance across a line (i.e., normal to the line). This value is often specified for circuitry artwork lines to regulate or check the actual or the artwork image produced from a computer plot or other image master.

**GEOMETRY TYPE** - [R] A classification of the basic geometry such as Line, Arc, and Polygon.

**GLAZE** - [R] An insulating film material used to protect underlying circuitry.

**HYBRID ASSEMBLY COMPONENT** - [R] A product or an assembly which has been identified and located within a hybrid assembly.

**HYBRID CAD PRESENTATION** - [R] The design file that contains the electronically coded data available on a particular hybrid design.

**HYBRID ID** - [R] All information needed to uniquely identify a particular product, manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, case style, and other product notation.

**HYBRID MICROCIRCUIT ASSEMBLY (HMA)** - In general an integrated circuit that is not monolithic. The term hybrid denotes that the circuit elements are made by two or more different technologies. A typical hybrid may consist of semiconductor chips and capacitors attached to a ceramic substrate with printed resistors and interconnections which are screen printed and fired.

**HYBRID NAME** - [R] A descriptive name given to a hybrid that usually describes its function.

**HYBRID NUMBER** - [R] The product number of a particular hybrid type.

**HYBRID SUBSTITUTE PART NUMBER** - [R] Other organizations identification (i.e., the customer may have alternate product number for the same hybrid).

**HYBRID VERSION** - [R] The revision level of a hybrid; each change to the hybrid design results in a new hybrid Version.

**LAND** - [R] A portion of a conductive pattern usually used for electrical connection, component attachment, or both.

**LAYER** - A strata of material such as conductor, dielectric, or resistor material which forms part of the hybrid structure.

**LAYER DISPLAY COLOR** - [R] The display color of a layer on a color drawing or on a CAD machine.

**LAYER NAME** - [R] The name of a particular layer (dielectric or conductive) such as Glaze or top conductor.

**LAYER SEQUENCE NUMBER** - [R] A particular layer of material (conductor or dielectric) position on the hybrid substrate with respect to the first layer. Usually begins with the first material placed on a substrate. These layers relate to process layers as contrasted with e.g., CAD layer.

**LAYER TYPE** - [R] A category used to describe the function performed by a deposited layer such as Conductor, Dielectric, Fill, Glaze, Resistor, Epoxy, Solder.

**LAYER RESTRICTION** - [R] A design restriction which is imposed on a particular layer of the product.

**LEAD FRAME** - [R] The metallic portion of the device package that completes the electrical connection path from the die or substrate conductors to the external circuitry.

**LEAKAGE CURRENT** - [R] The flow of electrons through the dielectric of a capacitor, usually expressed as a maximum which will be acceptable for the component.

**LEVEL OF PREFERENCE** - [R] A relative rating assigned to a product in a collection of functionally similar products which indicates its ranking of desirability for use in a product to be produced for the rating organization.

**LIBRARY NAME** - [R] The name of part in CAD system files of part information.

**LINE RESISTANCE** - The resistance of a conductor line on a substrate measured in total trace resistance.

**LINE WIDTH** - [R] (See Geometry Line Width.)

**LOG REQUIREMENTS** - [R] Indicates what information about the process step must be recorded and retained such as Machine ID, Component Lot Identification, Start Time, Stop Time.

**LOSS FACTOR** - [R] A property of an insulating material that is equal to the product of its dissipation and dielectric constant.

**MANUFACTURER NAME** - [R] The name a company is registered to do business under; may also include a company division name.

**MAX SUBSTRATE SIZE** - [R] The largest size of substrate which can be accommodated.

**MIL** - [R] A unit equal to 0.0254 millimeter (mm), (or 0.001 in).

**MOUNTING PAD** - [R] Metallization pattern on the substrate associated with a component for

the purpose of indicating the region for physical attachment of the component to the substrate. See Attach Material Pattern.

**MULTICHIP MODULE** - [A] A complex multilayer circuit containing components (integrated circuit chips) which cover at least half of the available circuit area. Note that this term is not present in the CAD information.

**MULTI-UP ID** - [R] The unique identification of data which indicates the placement of an array of images nested together on a single photo tool artwork. For files containing product information, the identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, and other product notation.

**NET** - An entire sequence of electrical connections from the first source point to the last target point, including lands and vias. The Net is identified by a Net Name which is unique within the product, and may also have a signal name.

**NET DESIGN RULE** - [R] Specified constraints on parameters related to the connectivity. Examples are maximum distributed inductance, or maximum circuit length.

**NET DESIGN RULE NAME** - [R] The assigned identification of a specification for some parameter of all conductive elements associated with an individual signal.

**NET DESIGN RULE VALUE** - [R] The measurement allocated to some parameter of all conductive elements associated with an individual signal.

**NETLIST** - A to-from listing of all the interconnections in the design. The netlist should correspond to the to-from listing of all the wires in the schematic. (Model; set of Net.)

**NET NAME** - A character string used to identify and distinguish nets; the name of the logical connection realized by the trace.

**OBSTRUCTION** - A physical entity which restricts where a component or a trace can be placed. See also Component Placement Restriction.

**ORIENTATION** - [R] The angle of rotation of a component relative to a predetermined direction.

**PACKAGE** - An integrated circuit, or a hybrid circuit. It provides hermetic or nonhermetic protection, determines the form factor, and serves as the first-level interconnection externally for the device by means of package terminals.

**PACKAGE DIMENSION** - The physical measurements of the package. See Part Outline.

**PACKAGE ID** - [R] The unique identification of a component enclosure. For files containing product information, The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, case style, and other product notation (e.g., TO-18; a JEDIC Standard number for a metal transistor package).

**PACKAGE OUTLINE** - [R] The 3-dimensional curve and surface geometry of a component package.

**PACKAGE PIN LOCATION** - [R] The geometric position of a lead in a part package of an electrical product with respect to the part origin and reference axis.

**PACKAGE PIN NAME** - [R] A referencing word that describes a use for the lead of a component package; such as "Output1".

**PACKAGE PIN NUMBER** - [R] The identifying number assigned to the lead of a package for

electronic components.

**PACKAGE PIN TYPE** - [R] The name given to the lead of a component package which indicates how the lead is to be attached to the assembly.

**PAD** - The metallized area on a substrate or on the face of an integrated circuit used for making electrical connections. Also see land.

**PAD END FEATURE** - [R] The type of joint formed on a wirebond wire at the place where the wire attaches to the circuitry of an assembly.

**PAD TYPE** - [R] The descriptive name that implies the function of a pad.

**PADSTACK** [I] - An ECAD construct for all of the pieces of information (features) about a component pin needed to establish the interconnection /layer geometry on the hybrid.

**PAD WIREBOND END FEATURE** - [R] The method of attaching a wirebond to a pad as denoted by the appearance of the joint such as wedge, ball.

**PANEL MULTI-UP** - [R] Multiple of the same image on one piece of material that will be separated after processing into multiple substrates

**PART** - [A, R, I] An individual functional element in a physically independent body that cannot be reduced or divided without destroying its stated function. When assembled onto the completed film network will form part of the circuit assembly. In a CAD system, represented as a graphic symbol with attached annotations. Parts are manufactured items; the information about which is usually stored in a library or listed in a catalogue.

**PART GRAPHIC**- [R] The graphic presentation of a component.

**PART ID** - [R] All information needed to uniquely identify a particular item, manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, case style, and other product notation.

**PART KIND** - [R] A category of component describing how it is used electrically such as mechanical, passive, active.

**PART MANUFACTURERS NAME** - [R] The corporate name used by the manufacturer of components.

**PART NAME** - [R] Description of the function of the component such as Coil, Cover, IC Chip, Transistor, Resistor Header, Substrate.

**PART OUTLINE** - [R] The boundary of component on the top assembly drawing or the CAD equivalent.

**PART PROPERTY** - [R] A pair of terms, one indicating the property name (see Component Property Name), the other the value of the property (see Component Property Value).

**PART PROPERTY NAME** - [R] The name of a measured parameter associated with a device used in an assembly. Examples are capacitance, inductance, gain, resistance, and temperature range.

**PART PROPERTY VALUE** - [R] The value associated with a Component Property. Examples would be 10K as a value for the resistance property, or 50 as a value for the low frequency gain property of a semiconductor.

**PASSIVE COMPONENT** - [R] A component which does not exhibit signal gain but does affect one or more other parameters of a signal. Examples are resistor, inductor, and capacitor.

**PATH VERTEX** - The X, Y location which specifies one end point of the linear segment of a trace.

**PATTERN** [R]- The configuration of materials on a panel or printed board layer. Pattern also denotes the circuit configuration on related tools, drawings, and artwork masters.

**PATTERN ID** - [R] The unique identification for the artwork for a specified layer of a laminated product.

**PATTERN VALUE** - [R] The measurement value assigned to a deposited or etched component at some specified stage in the fabrication cycle. An example is 2300 ohms prior to trimming.

**PATTERN VALUE MIN & MAX** - [R] The tolerance associated to the deposited or etched component.

**PHOTOLITHOGRAPHY** [A]- The use of light or ultraviolet rays through a mask to define circuit conductor patterns. (Model; intractable taxonomy.)

**PHOTOPLOT APERTURE**- Mechanism which allow a certain amount and incidence of light to expose film, thereby making a "photograph" of design being plotted. See Aperture Size.

**PHOTORESIST** [A]- A photosensitive coating that is applied to a laminate and subsequently exposed through a photo tool (film) and developed to create a pattern that can be either plated or etched.

**PHYSICAL LAYER** (1 top) - A conductor, dielectric, or fill for each layer.

**PIN** - The identification of a possible connection to a component providing a reference point for creating a netlist.

**PIN ASSIGNMENT** - [R] The name of the characteristic or electronic function assigned to the lead of a component package in a circuit.

**PIN END FEATURE** - [R] The type of joint formed on a wirebond wire at the place where the wire attaches to a component.

**PIN LOCATION** - The physical location of pins on a component package with reference to its assembly origin.

**PIN NAME** - [R] The general functional notation for the signal role at the lead of a component package such as E, B, C on a transistor.

**PIN NUMBER** - A number used to distinguish pins on a component or package.

**PIN TYPE** - The name of a characteristic on a pin, such as input, output, tri-state analog.

**PIN WIREBOND END FEATURE** - [R] The characteristic of the wire at a joint with the material to which the wire is attached. The usual characteristics given are wedge or ball.

**PLACEMENT NAME/PHYSICAL NAME** - The name of component in CAD library.

**PLACEMENT TOLERANCE** - [R] The permitted positional variation of a component on an assembly.

**PLATING** - (1) The metallic deposit on a surface, formed either chemically or electrochemically. (2) the process of the chemical or electrochemical deposition of metal on a surface. (Model;

Deposition taxonomy.)

POINT - [R] A singular location in a given coordinate system.

POINT X VALUE - [R] The numeric value in one (usually horizontal when viewed from a reference coordinate system) direction from a single point spatial reference.

POINT Y VALUE - [R] The numeric value of a single point reference, in a direction orthogonal to the x vector direction.

POWER DENSITY - [R] A measure of the concentration of energy, such as 1 watt per square inch.

POWER DISSIPATION - (T50) [R] In watts/meter<sup>2</sup> (heat flux density), the energy used by an electronic device in the performance of its function.

PREFORM - [R] For soldering or adhesion functions, a form which is punched out of thin sheets of solder, epoxy, or eutectic alloy. The form is placed on the spot of attachment by soldering or by bonding prior to placing the object there to be heated. (a type of Part Name)

PRIMITIVE TYPE - [R] The category of simple geometric element that makes up artwork such as geometry or text.

PROBE PAD - A connection point for an external probe used to test some aspect of the hybrid circuit function. For example, a probe pad may be used to make connections to a screened resistor during the trimming process.

PROCEDURE - [R] A step-by-step description of the activities needed to complete a given operation.

PROCESS ID - [R] The unique identification of the parameters used on one process step during manufacturing. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, and other product notation.

PROCESSING CONSUMABLE - [R] Material or chemicals which are used in manufacturing processes which do not remain as part of the product being manufactured. Examples include cleaning fluids, flux, and photoresists.

PROCESS DESCRIPTION - [R] The narrative explanation of an identified step in the fabrication of a product or assembly.

PROCESS OPERATION - [R] The procedures sequentially described by a document identified by the Process ID.

PROCESS STEP - [R] A single operation used to manufacture an Assembly Occurrence. Each step corresponds to one block on a flow chart.

PROCESS STEP NUMBER - [R] A sequential number assigned to a process step.

PROCESS VARIABLE NAME - [R] The identifier assigned to a particular fabrication step.

PROCESSING CONSUMABLE NAME - [R] The generic identification of a substance used during the fabrication of a product or assembly, but which does not remain as part of the product. Examples are flux, solvent, or resist.

PRODUCT CONSUMABLE - [R] Material or chemicals which are used in manufacturing processes and which remain as part of the product being manufactured. Examples include solder, epoxy, and plated metals.

**PRODUCT CONSUMABLE NAME** - [R] The generic name of material or chemicals which is used in manufacturing processes and which remain as part of the product being manufactured.

**PRODUCT TOLERANCE** - [R] The allowable deviation from the specified location of a product feature.

**PRODUCTION TOLERANCE** - [R] The allowable deviation from the specified location of a product feature.

**PROGRAM** - [R] A text string indicating the system a hybrid was designed for or intended to be used in.

**QUALIFIED VENDOR** - [R] A company from which components are purchased and which has been identified as meeting specified requirements for certification and/or inspection of the components being sold.

**REFERENCE DESIGNATOR** - [R] A character string which defines an instance of an assembly component; unique within the hybrid. The guidelines generally followed are found in ANSI Y32.16-1975 (e.g., R1=Resistor 1, U7=Microcircuit 7, A10= Assembly 10; thus A10R6 is the 6th Resistor in Assembly 10).

**REGISTRATION** - The proper alignment of layers with respect to other layers or to the substrate. The accuracy of registration is measured as the concentricity or relative position to a datum.

**REGISTRATION MARK** - [A, R] The marks on a wafer or substrate that are used for aligning successive processing masks. Also known as alignment marks or fiducial marks.

**REGISTRATION MARK NAME** - [R] The term assigned to a locating orientation feature related to a particular use.

**RESISTIVITY** - The ability of a material to resist the passage of electric current. See also Resistor, Sheet Resistance or Line Resistance.

**RESISTOR** - A device that offers resistance to the flow of electric current in accordance with Ohm's law:  $R = E/I$ , where R is resistance, E is voltage, and I is current.

**RESISTOR GEOMETRY** - The film resistor outline. The four system generated geometries for many CAD systems are as follows: rectangle, tophat, u - shaped, serpentine.

**RESISTOR MAX ASPECT RATIO** - A greatest-value factor obtained by dividing the specified width by the length and multiplying the numerator and denominator by a constant such that the resulting factor is a simple number, such as 4:1. Such a design rule may constrain the automated design system, and is transferred with the design. The rule is not necessarily intended to be applied to the finished product.

**RESISTOR MIN ASPECT RATIO** - A least-value factor obtained by dividing the specified width by the length and multiplying the numerator and denominator by a constant such that the resulting factor is a simple number, such as 1:6. Such a design rule may constrain the automated design system, and is transferred with the design. The rule is not necessarily intended to be applied to the finished product.

**RESISTOR MIN LENGTH** - A design rule—or metric—which establishes the least acceptable dimension a resistance trace length, such as 40 mil. Such a design rule may constrain the automated design system, and is transferred with the design. The rule is not necessarily intended to be applied

to the finished product.

**RESISTOR MIN WIDTH** - A design rule—or metric—which establishes the least acceptable dimension across a resistance trace, such as 20 mil. Such a design rule may constrain the automated design system, and is transferred with the design. The rule is not necessarily intended to be applied to the finished product.

**RESISTOR OVERLAP** - A thick-film conductor pad that overlaps and makes contact with a thick-film resistor area.

**RESISTOR PASTE VALUE** - [R] Material used to create thick film resistors rated with a nominal ohm per square value.

**RESISTOR SHAPE** - [R] The term which is characteristic of the topology used for a deposited or etched resistor component.

**RESISTOR TERMINATION** - The contact area between a thick- or thin-film resistor and an adjacent conductor layer.

**REVISION** - [R] Number(s) and/or character(s) that uniquely identify a version of documentation and the products built to that documentation.

**ROUTE REGION** - (T50) Region where routing paths can automatically be placed between points to be interconnected.

**SCHEMATIC** - (T50) A drawing that shows, by means of graphic symbols, the electrical connections, components, and functions of a specific circuit arrangement.

**SCHEMATIC ID** - [R] All information needed to uniquely identify a particular circuit functional diagram, manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, case style, and other product notation.

**SCREEN ID** - [R] All information needed to uniquely identify a particular screen, manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, and other product notation.

**SCREEN PRINTING** - [A] A process for depositing material in a pre-defined pattern by forcing material through a stencil screen with a squeegee.

**SCREEN STENCIL** - [A] A network of metal or fabric strands, mounted snugly on a frame, and upon which the film circuit pattern and configurations are superimposed by photographic means. (from ISHM Industry Guide, 1990)

**SHEET RESISTIVITY** - [R] Electrical resistance of a thin sheet of a material with a uniform thickness as measured across opposite sides of a unit square pattern expressed in ohms per square. (from ISHM Industry Guide, 1990)

**SIGNAL CONDUCTIVE PATTERN** - [R] The association of geometry and the electrical characteristic that is intended to be carried on the material finished to that geometric shape.

**SIGNAL NAME** - [R] The user defined functional name, usually referring to an electrical impulse of predetermined voltage, current, polarity, and pulse width. See also Net Name.

**SOLDERING** [A]- A process of joining metallic surfaces by melting solder.

**SPECIFIED TOLERANCE** - [R] The amount of (usually) dimensional deviation which has been

called for in the product specification.

**START LAYER - [R]** The first of one or more layers through which a via or passage will pass.

**STATION - [R]** The place or the equipment which is identified (in planning) as the location of a processing or an assembly step during the manufacturing of a product.

**STEP X COUNT - [R]** The number of patterns in X direction in panel multi-up.

**STEP X DISTANCE - [R]** The X step distance between patterns in panel multi-up.

**STEP Y COUNT - [R]** Number of patterns in Y direction in panel multi-up.

**STEP Y DISTANCE - [R]** The Y step distance between patterns in panel multi-up.

**STOP LAYER - [R]** The last layer through which a via or passage will pass.

**SUBSTRATE [R]-** The supporting structural material into and/or upon which the passivation, metallization and circuit elements are placed. MIL-STD-883C (Usually aluminum oxide (alumina)).

**SUBSTRATE OUTLINE [R]-** The graphical representation of the substrate shape.

**SUBSTRATE MATERIAL - [R]** The name of the substance from which the base layer is formed.

**SUBSTRATE THICKNESS - [R]** The nominal material cross section of the base material of a laminated product.

**SURFACE RESISTIVITY - [R]** (See Sheet Resistivity.)

**SWAPPING - [A]** The process that exchanges connections from one pin to another pin to improve routing, provided the pins are in the same gate and in the same swap group.

**TEMPERATURE COEFFICIENT OF CAPACITANCE - [R]** A multiplier which represents the linear change of a capacitance value per degree change in temperature. It may be positive, negative, or zero and is usually expressed in parts per million per degree Celsius, or  $10^{-6}$ .

**TEMPERATURE COEFFICIENT OF RESISTANCE - [R]** A multiplier which represents the linear change of a resistance value per degree change in temperature. It may be positive, negative, or zero and is usually expressed in parts per million per degree Celsius, or  $10^{-6}$ .

**TERMINATOR MOUNTING - [A]** Metallization pattern on the substrate associated with a film component. The purpose of the pattern is to indicate the region for electrical connection of the film component to its connecting traces.

**TEST - [R] [A]** The examination of a product during or after fabrication for conformance to specified criteria for that product.

**TEST CONDITION - [R]** The specification of the setup needed to carry out a specific test of a product. Examples include supply voltage, temperature, and initializing signals.

**TEST DESCRIPTION - [R]** The narrative which is followed in performing the specified test.

**TEST MAXIMUM - [R]** Value of the upper limit of a range of test values.

**TEST MINIMUM - [R]** Value of the lower limit of a range of test values.

**TEST SEQUENCE NUMBER - [R]** A number assigned to a test in a series of tests.

**TEST SYMBOL - [R]** Short character sequence that allows easy reference to test such as Vin.

**TEST TOLERANCE - [R]** The acceptable deviation from the specified test results parameter.

TEST TYPE - [R] Category of test being performed such as Final, Pre-burn, Qual, Sample.

TEST UNITS - [R] Measurement units of the Test Minimum and Test Maximum values for the test.

TEXT - [R] An ordered sequence of characters (glyphs) to which a meaning is ascribed.

TEXT ATTRIBUTE - [R] The characteristics that describe the appearance of text such as size, font, slant, layer.

THERMOCOMPRESSION BONDING - [R] The process involving the use of temperature and pressure to join two materials by interdiffusion across a boundary. (from ISHM Industry Guide, 1990)

THERMOSONIC BONDING - [R] The process involving the use of temperature, pressure and applied ultrasonic energy to join two materials by interdiffusion across a boundary. (from ISHM Industry Guide, 1990)

THICK-FILM CIRCUIT - [R] A circuit that is fabricated by the deposition of paste materials such as screen-printed ceramic material (cermet) pastes on a ceramic substrate, which are fired in a kiln to create permanent circuit patterns.

TOOL - [R] (See Tool Type.)

TOOL DESCRIPTION - [R] A narrative which indicates the use of the implement.

TOOL ID - [R] All information needed to identify uniquely a particular manufacturing implement—manufactured in-house or purchased. The identification may include, but is not limited to, the Drawing Number, Revision, Revision Status, Dash Number, Cage Number, and other product notation.

TOOL TYPE - [R] The name given to a device used, as part of product manufacturing, to accomplish an operation. Examples include the product traveler, a cutting device, or a machine.

THIN-FILM CIRCUIT - [R] Conductive, resistive, or dielectric material, usually less than 50,000 angstroms in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means. (from MIL-STD-883C, Notice 12)

TRACE KEEPOUT - [R] Symbolic representation of a region (layer-specific) associated with component which may not be used for trace routing.

TRACE LAYER - [R] The physical layer on which the given trace exists.

TRACE WIDTH - [R] The physical width of the trace segment. The width data is typically used to control the photoplotter aperture or the pattern generator setting.

TRACE WIDTH TOLERANCE - [R] The allowable range of the dimension across a conductive line.

TRIM PATH - [R] The path made by trimming (using an abrasive or a laser) a component to obtain the design value.

UNITS (e.g., Volt, Meter) - [R] A definite amount or quantity used as a standard of measurement.

USER DEFINED PROPERTIES - [I] Structured data describing information that is not previously defined. This property is often used for information not yet defined for the data structure.

**USER INFORMATION** - [R] Unstructured text information inserted as user comments, such as drawing notes.

**VACUUM DEPOSITION** - The deposition of a metal film onto a substrate in a vacuum by metal evaporation techniques.

**VARIABLE VALUE** - [R] Quantitative data that is associated to a particular named data element.

**VENDOR ADDRESS** - [R] The postal location of the organization from which items are procured.

**VENDOR NAME** - [R] The identifying text of the company, which may include the company division, that supplied materials, equipment, or service.

**VIA HOLE** - [R] A hole (i.e., a void or passage) through insulating layer (s) used to make a connection (electrical or thermal), but for which there is no intention to insert a component lead or other reinforcing material. The hole may be any shape as defined by a Via Shape.

**VIA KEEP OUT** - [R] The symbolic representation of a region (layer-specific) associated with a via where traces cannot exist.

**VIA LAYER** - [R] A layer which is used principally (in a CAD system) for placing vias holes.

**VIA LOCATION** - [R] The X, Y position on which a via is positioned.

**VIA SHAPE** - [R] The shape of the top view of a via.

**VIA SIZE** - [R] The width and length or the diameter of a via.

**VOLTAGE ALLOWANCE** - [R] A design rule that requires extra spacing between specified traces (e.g., to allow higher voltages to be carried).

**VOLUME RESISTIVITY** - [R] The volume resistance between two electrodes (of unit area and unit distance apart) that are in contact with or embedded in a specimen. The value is the ratio of the direct voltage applied to the electrodes in proportion to the current between them that is distributed through the volume of the specimen. Usually expressed in ohms per centimeter.

**WIRE BOND** - [A, R] A completed wire connection that provides electrical continuity. Bonding wires are used to connect between component pads, or package pin, or conductive pads on the hybrid substrate.

**WIRE BOND MAX LENGTH** - [R] A design rule—or metric—to limit total length of a wirebond wire, such as 140 mils maximum.

**WIRE BOND MIN LENGTH** - [R] A design rule—or metric—to limit the least-length parameter of a wirebond wire, such as 10 mils minimum.

**WIRE BONDING** - [A] The method used to attach very fine wire to make electrical connections.

**WIREBOND SEQUENCE NUMBER** - [R] The number assigned to a wirebond that specifies the order in which wirebond is to be made.

**WIRE SIZE** - [R] The diameter of wire, such as 0.8, 1, 5 mils.



## 4. INFORMATION REQUIREMENTS AND APPLICATION REFERENCE MODEL

In this section, hybrid product information needed for the documentation and manufacture of the end item is described in the Application Reference Model (ARM). In addition, the task of identifying collections (or groupings) of information, termed “units of functionality” or UoFs, are assembled into categories and described in section 4.1. In section 4.2.1, the methodology used to convey information and the method's implied constraints, are described. Lastly, in section 4.3, the results of utilizing the method to capture all of the data entities (i.e., information primitives) as they relate to each other are diagrammed.

It should be noted that information that describes the logical information structures required for accomplishing the physical implementation of an associated Application Reference Model is called an Application Interpreted Model (AIM) and is found in section 5. The indication of when the information is used during the overall design and manufacturing process is documented in the Application Activity Model (AAM) in Appendix A.

### 4.1. Units of Functionality (UoF)

A single hybrid design file can be used as the source for several different kinds of processes. For hybrid microcircuit applications, these processes can be functionally grouped within three general categories. Each category recognizes a different end use for the hybrid design, and each category can be further divided into units of information. These units of information within each of the categories are called Units of Functionally (UoF). Each independent entity in the ARM constitutes a UoF. Further, the child entities of these entities may, together with their existence-dependent entities, be used in a UoF structure. For a view of the relationships between categories, Units of Functionally, and entities, see table 1. The symbol “+” indicates that all child entities apply as well.

Although it is possible to establish a wide variety of categories, each oriented differently and each perhaps varying in detail, for the purposes of this version of the AP, three functionality categories are defined:

1. Documenting Drawing; used for the control of hybrid procurement. The drawing contains information and graphics defining the desired package size and shape, the netlist or pin-signal information, the testing waveforms and test conditions, and the environment range over which the hybrid must function. Additional text supplies quality and procurement information.
2. Photolithography; the information which results in masks or artwork used for layer depositions or etching.
3. Machine Control; the information which guides the tools into position and controls the actions at that location. Examples are wirebonders and component placement machines.

The information for all three categories can originate in a computer aided design (CAD) system. Or part of the information for any category may be created by manual—non-CAD— means. The units of functionality defined herein are to be considered semantically constrained by this AP, and only the CAD information is (syntactically) constrained in the IGES form by the constructs in the

application interpretation model.

All functionality categories which have been originated in a CAD system are capable of being transmitted to another, or an intermediate CAD system. In this event, much of the information may be “exchanged” without distinction. For example, a design exchanged between CAD systems may adopt a level of information content that is greater than the Drawing. The receiving CAD system would benefit by “knowing” the properties and rules defined in the source system in addition to the product as a drawing graphic.

#### 4.1.1. Unit of Functionality Definitions

The definitions for general terms used in this section are found in section 3.1, and the glossary of data items of the ARM are found in section 3.2.

#### 4.1.2 UoF and ARM Correspondence

The hybrid product is defined in this AP by a combination of documents (called presentation) and CAD data (called representation). The CAD data consists of the screen display data and the product model itself. The ARM reflects the data distinction, where the three categories of functionality do not. For example, in Category 1 the hybrid product is defined through a drawing, such as a Specification Control Drawing. CAD systems may need only to produce a “paper document” intended for human interpretation. Information such as the hybrid schematic and waveforms are presently treated as such drawing data. Category 2 includes the CAD display information such as the color which a particular CAD-layer used. Category 3 is usually extracted from the CAD model of the product.

Each independent entity in the ARM constitutes a unit of functionality. Further, the child entities of these entities may, together with their existence-dependent entities, be used in a UoF structure. For purposes of this AP, the following table indicates appropriate units and the entities in the ARM which are related. The symbol “+” indicates that all child entities apply as well.

**Table 1: UoF to ARM Entity Correspondence**

UoF	Cat.	ARM Entities
Bill of Materials	1	Component, Assembly Consumables, Substrate
Package	1	Device Package
Schematic	1	Hybrid Documentation +
Artwork	2	Artwork Geometry +
Padstack Definition	2	Area+, Flashed Geometry, Via Hole, Probe Pad
Panel	3	Panel MultiUp, Hybrid Microelectronic Assembly
Component	3	Hybrid Assembly Component
Wirebond	3	Pin +

## 4.2 Application Reference Model

The Application Reference Model was created to define the semantics (data and relationships) of all information needed for the manufacture and documentation of the end item hybrid. The model may relate to information which is not typically captured during design. Examples are the test environment (text) supplied in a procurement drawing, or the signatures per se found in the drawing title block. The model does not include data related to enterprise management or to the use of the hybrid.

### 4.2.1 Descriptions of the ARM Data Constructs

The following sub-sections define the methods and interpretation of the model to follow and are not intended to provide a tutorial on the subject. For further explanation of the syntax and methods the reader is directed to manuals, information, and tools references available from the IDEF-Users Group, 1900 Founders Drive, Kettering, OH 45420; telephone (513) 259-4702

#### 4.2.1.1 ARM Methods and Language

The ARM is presented in the IDEF<sub>1</sub>X language. IDEF derives its name from the activity that developed the methodology, the Air Force Computer Aided Manufacturing (ICAM) Definition Program. The program developed several languages. IDEF<sub>1</sub>X, was developed to model data—the semantics of information. A data model may be considered as a *connecting link* between the user's view of the data (referred to as the external schema) and the manner in which the data is stored in a computer, or database (the internal schema). Common to these two views of the data is a conceptual schema and the data model is the visual presentation of the conceptual schema. In general, the data model is presented as a series of drawings that contain diagrams and accompanying text. The text forms a glossary that defines the terms used in the diagrams and more fully explains their relationships and context.

The component parts of an IDEF data model are the entities, their attributes and their relationships as illustrated in figure 4-1. An entity is an item (an object or an event) about which we wish to keep data. In general rectangles are used to graphically represent entities. If the entity is not within the scope of the present model, the outline of the entity is dashed, notifying the reader to look elsewhere for the definition of the entity. Each entity box has a name (the entity-class label) that is given above the rectangle and which is defined in the model glossary.

Attributes of an entity are shown inside the entity rectangle. An attribute will have one value (instance) for each instance of its entity. Some attributes that uniquely define the instance of an entity, called keys, are located above a line at the top of the entity rectangle. Keys are of several types and the general concepts of key migration follow those concepts as used to develop relational database structures. For example: the key attribute set from the parent entity is propagated downward through the model structure and such instances are called foreign keys. Attributes that are not keys are located below the horizontal line of the entity rectangle.

The relationships between entities is shown by the lines drawn between them in the model diagram. The relationship consists of the role and the cardinality. Text associated with the interconnecting lines provides a clear meaning (the role or predicate) of the relationship between the entities. One end of the line is connected to the entity rectangle denoting that this entity is the independent entity. At the other end of the line, the dependent entity end, a terminator symbol (a

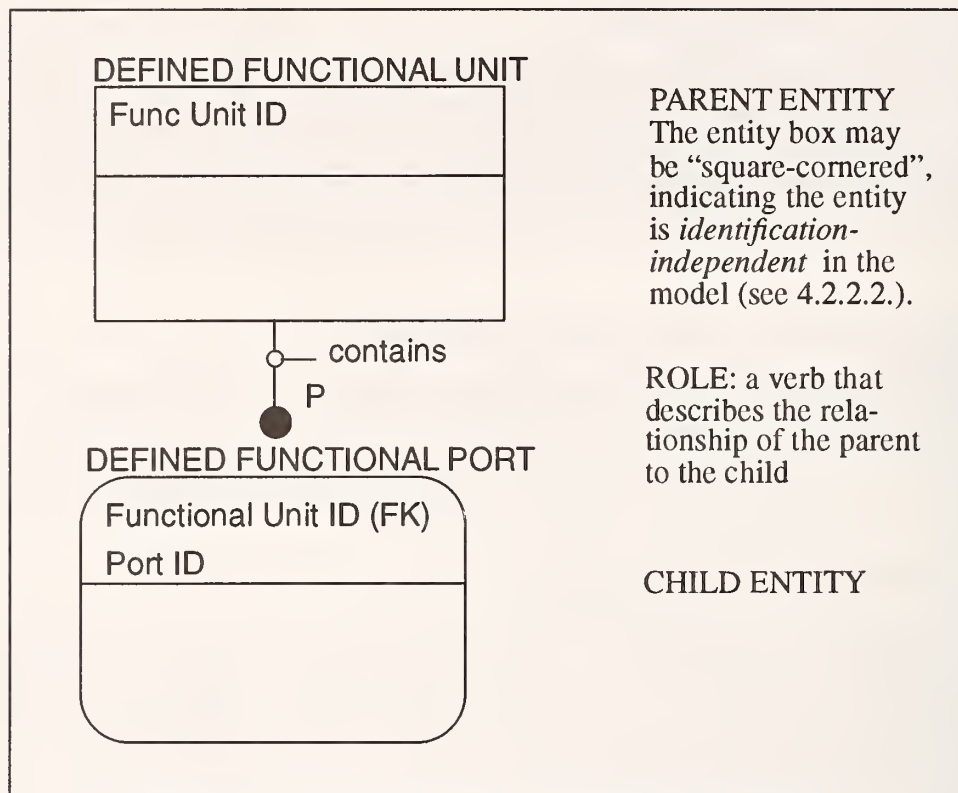


Figure 4-1. Component Parts of an IDEF Relationship.

"big dot") may carry cardinality information on how to read the model as in figure 4.2. If there is no letter adjacent to the terminator symbol, there may be "zero, one or many" entities associated with the relationship. Likewise, the letter Z designates "exactly zero or one," P designates "one or many," and the letter n designates some exact integer number of occurrences.

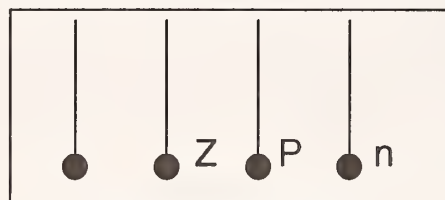


Figure 4-2. Cardinality.

Lastly, models may contain information that denote the "categorization" or types-of entities as diagramed in figure 4-3. Each instance of the generalization parent must be one of the types. A double horizontal bar indicates that all types of dependent entities are present (for example, all people are either male or female). If all of the various types of entities are not listed (the model equivalent to a written ellipsis (...)), then a single horizontal bar is used to show that there may be relationships not shown and the categorization is assumed to not be complete.

A related pair of entities are read, that is, retrieved as an English sentence, in the form of an assertion. The pair may be read in both directions. From the top down (i.e., toward the entity at the big dot end of the relation line), the set is read as the independent entity, the relation label, and

then the dependent entity. From the bottom up, the usual relation is “always has exactly one.”

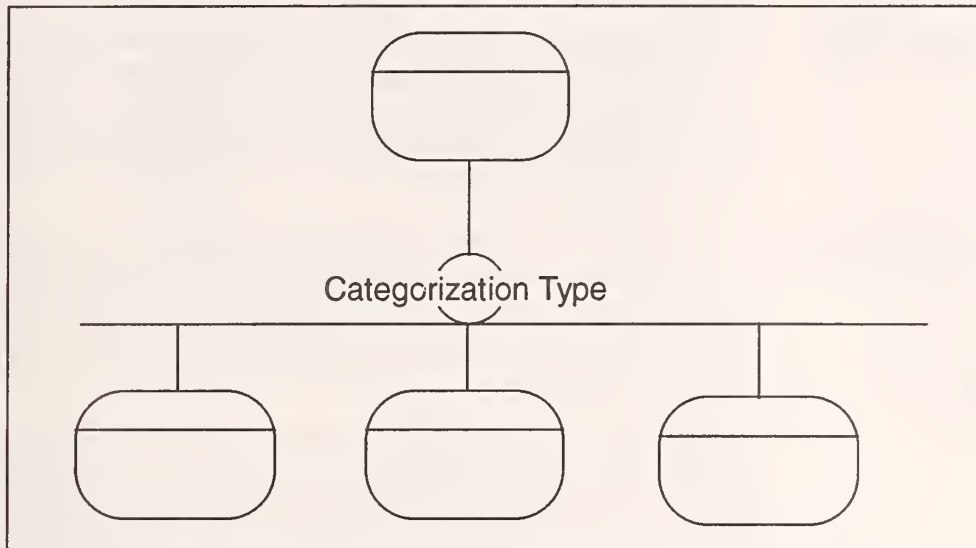


Figure 4-3. The Categorization Structure.

Additional details may be obtained that will enable those who are interested in working with IDEF to become more proficient at reading the models. Several good references are available.<sup>5, 6</sup>

## 4.2.2 Data Construct Definitions

The definitions of entities for the Hybrid Microcircuit ARM are found in section 3.2.

### 4.2.2.2 Data Construct Assertions

The method and language (IDEF<sub>1</sub>X) used for this AP ARM carries several assertions important to the interpretation and application of the ARM.

Attributes:	All attributes which appear within the entity box exist whenever an instance of the entity occurs, unless designated by the (null OK) notation.
Relationships:	The ARM is intended to be interpreted independently of any computer database structure. Thus the entities may be considered as representing objects in an Object Oriented (OO) system, or as tuples in a Relational system. As such, the keys have not been migrated as required by relational notation. The relationships (connecting lines)

<sup>5</sup>. Parks, Curtis H., “Tutorial: Reading and Reviewing the Common Schema for Electrical Design and Analysis,” presented at the 24<sup>th</sup> Design Automation Conference.

<sup>6</sup>. Loomis, Mary E. S., “Data Modeling - The IDEF<sub>1</sub>X Technique,” Proceedings of the IEEE, 1976 Phoenix Conference on Computers and Communications, Phoenix, AZ, (March 26-28, 1986) pp. 146-149.

may be used to define OO methods, or to migrate relational foreign keys. The entity at the *attached* end of a relationship line is considered the *parent* of the two entities. The following dependencies apply to the parent-child relation.

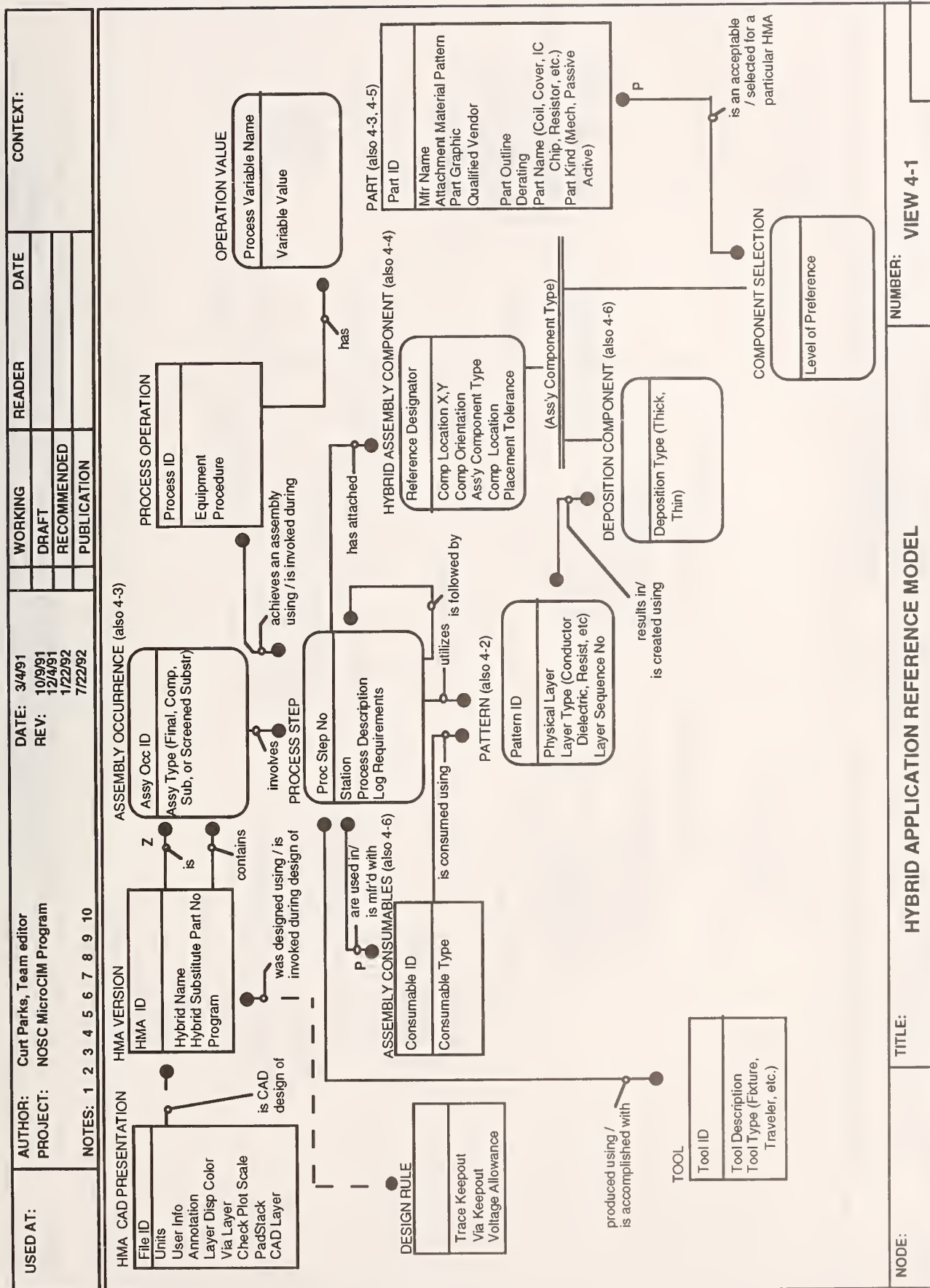
**Existence Dependencies:** The existence of a relationship (line) indicates that, should an instance of the child entity exist (at the “cardinality” end), the related parent must exist. An example of this dependency from the ARM is that: A Layer instance cannot exist unless a Hybrid Microcircuit Assembly Version exists.

**Identification Dependencies:** In addition to the existence dependency above, if the relationship is a solid line, the unique identification of the child requires the key of the parent in addition to the key declared in the child. An example is the Layer instance can only be uniquely identified by knowing the hybrid it “belongs” to.

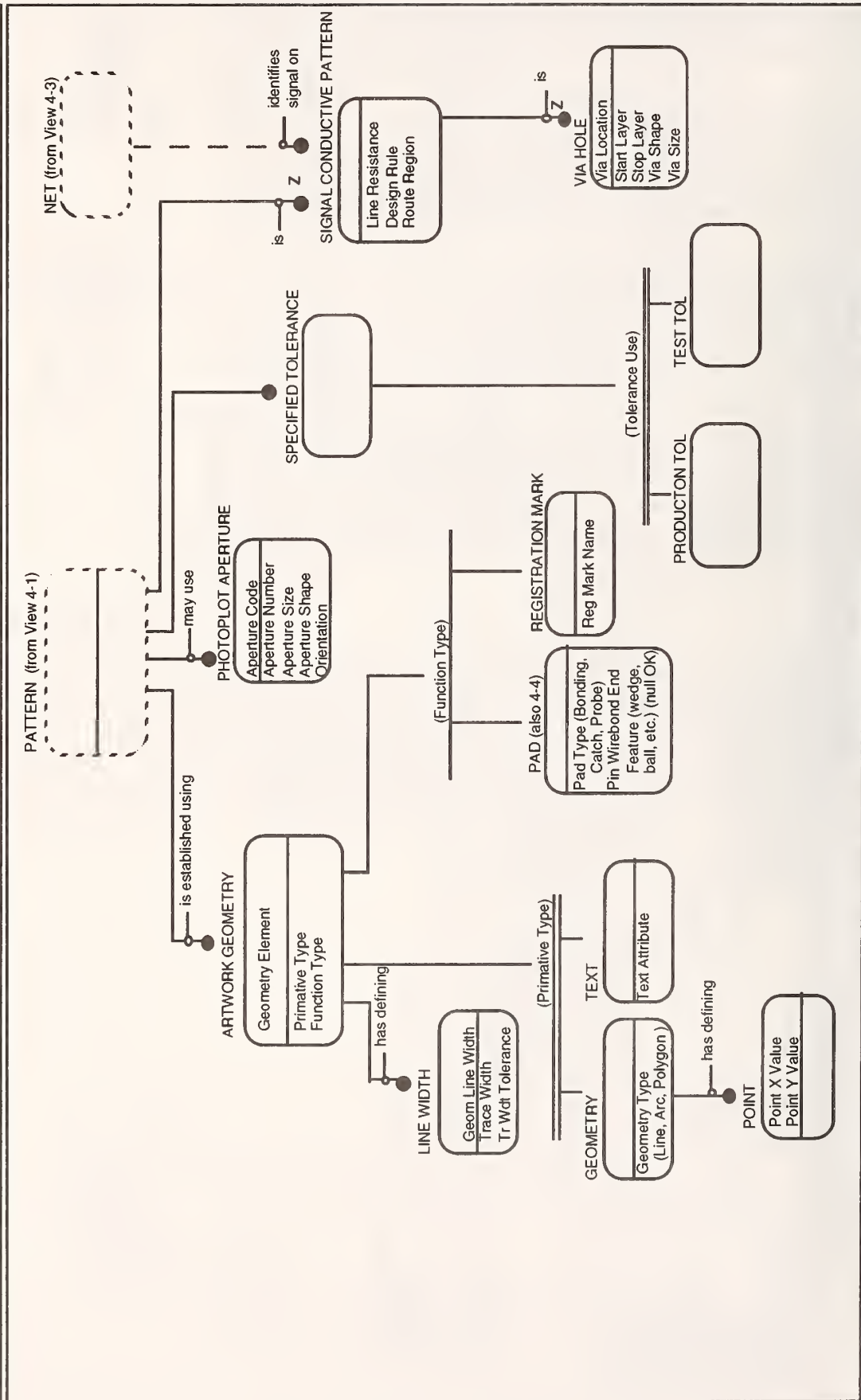
Round corners are used on an entity-box to indicate that there exists a parent entity which provides some of the key for identification. For entity-boxes with square corners, all of the entity’s key is owned by the entity; the entity exists independently within the given domain of the model.

### 4.2.3 ARM Diagrams

The ARM is intended to be an enterprise-view of the information about the hybrid as a product. The ARM serves as a reference-point for the data implementation as captured in drawings, in the CAD system, and specified for IGES exchange in the next section. The ARM diagrams (views) constitute an information model that documents the information structures needed to support the activities in the Application Activity Model (AAM) and to develop the corresponding IGES Application Interpreted Model (AIM).

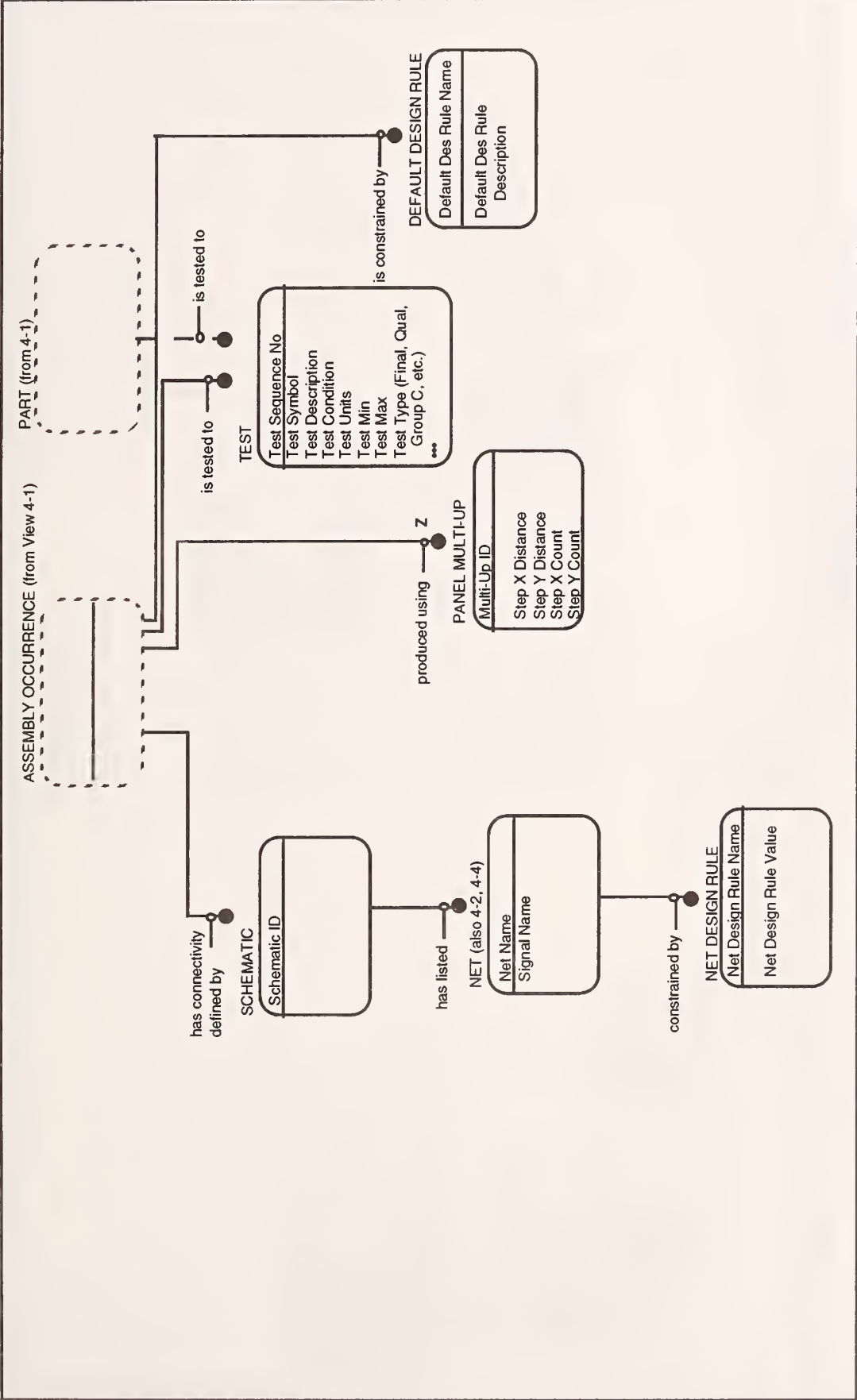


USED AT:	AUTHOR:	Curt Parks, Team editor	DATE:	3/28/91	WORKING	READER	DATE	CONTEXT:	
	PROJECT:	NOSC MicroCIM Program	REV:	10/9/91	DRAFT				
				12/4/91	RECOMMENDED				
				1/22/92	PUBLICATION				
NOTES:		1 2 3 4 5 6 7 8 9 10							



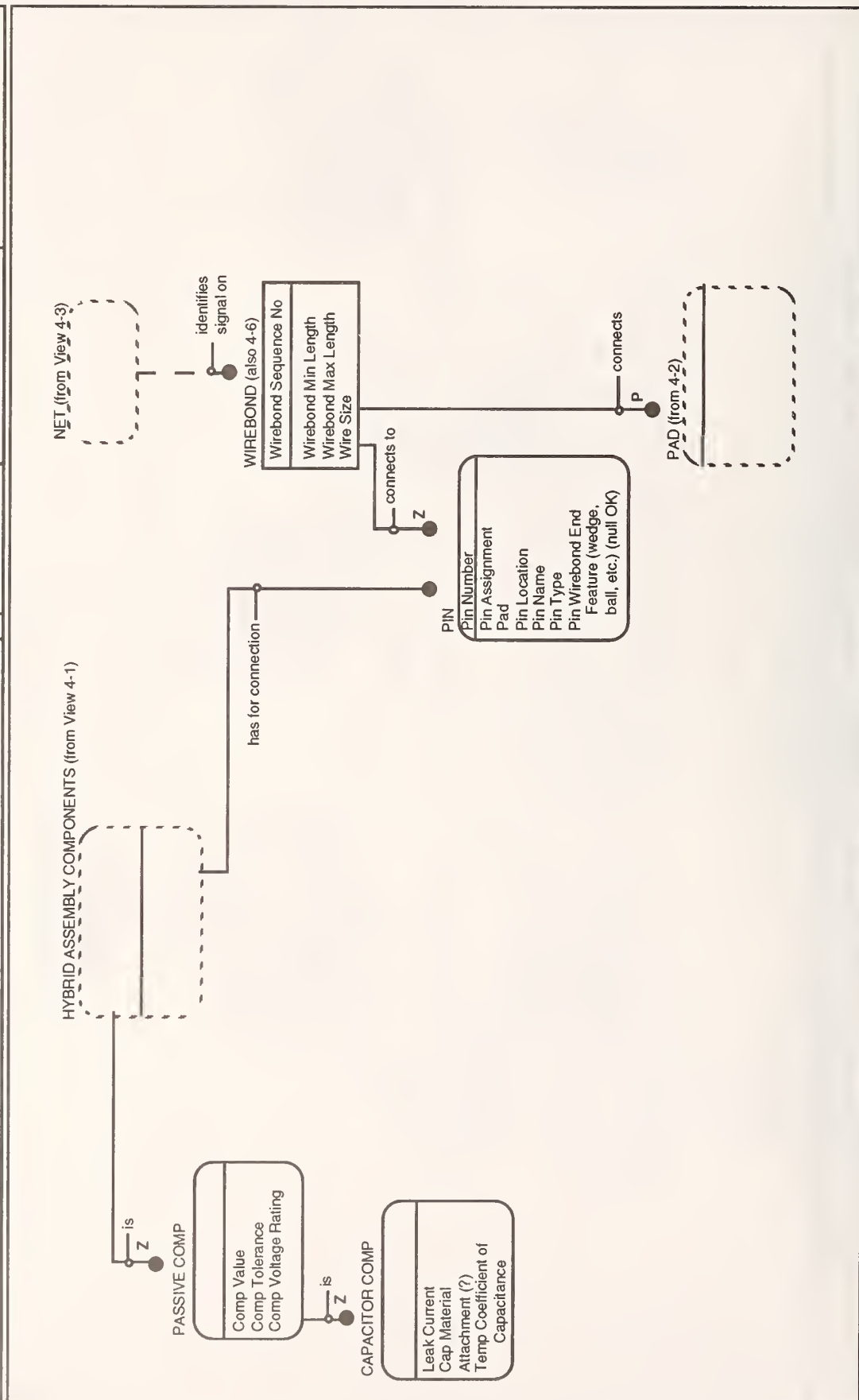
NODE:	TITLE:	HYBRID APPLICATION REFERENCE MODEL EXPANDED DEPENDENTS OF PATTERN	NUMBER:	VIEW 4-2
-------	--------	--	---------	----------

USED AT:	AUTHOR: Curt Parks, Team editor PROJECT: NOSC MicroCIM Program	DATE: 10/5/91	WORKING	READER	DATE	CONTEXT:
		REV: 12/4/91	DRAFT			
		1/22/92	RECOMMENDED			
		7/22/92	PUBLICATION			
NOTES: 1 2 3 4 5 6 7 8 9 10						



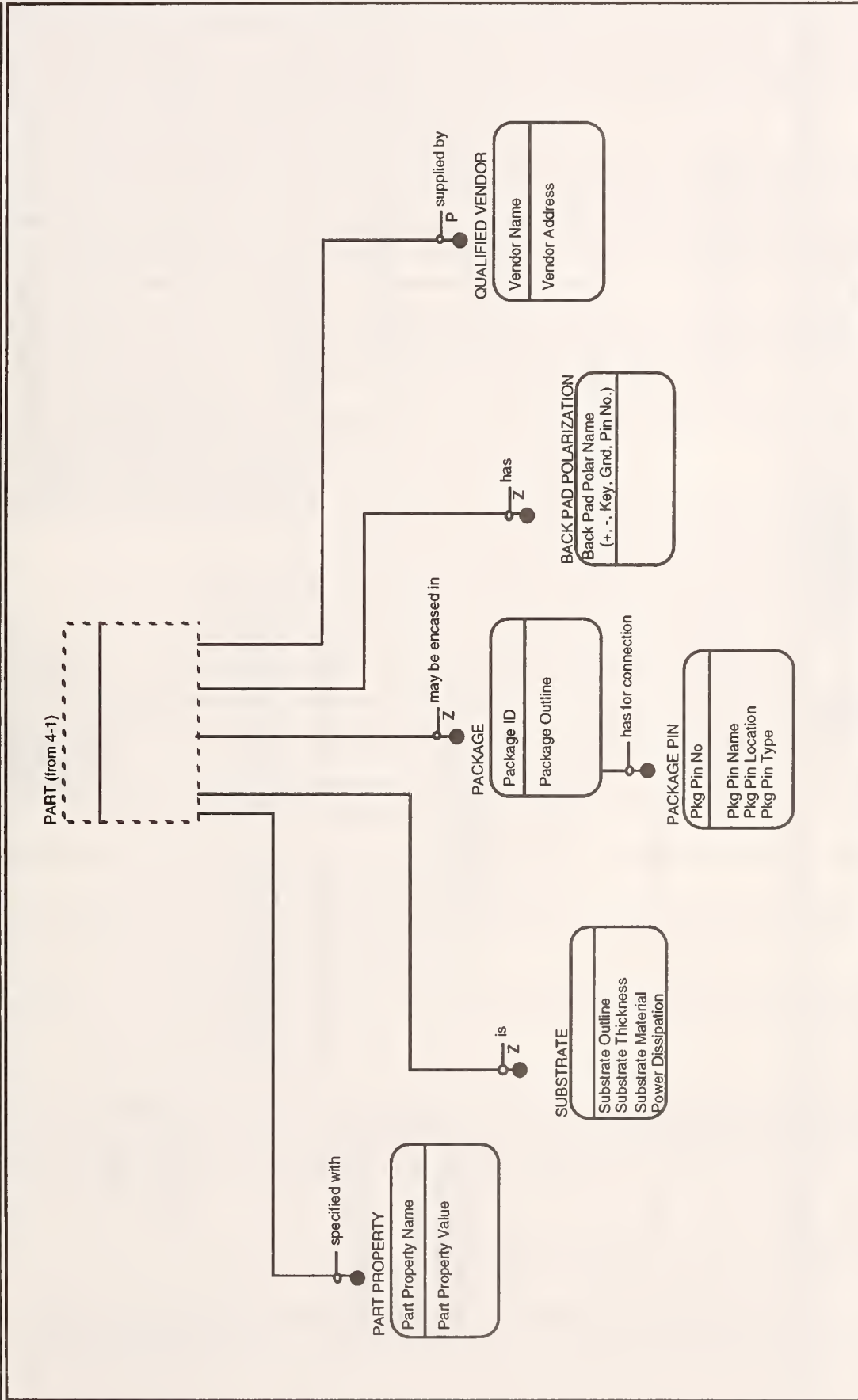
NODE:	TITLE:	NUMBER:	VIEW 4-3
HYBRID APPLICATION REFERENCE MODEL EXPANDED DEPENDENTS OF HYBRID VERSION			

USED AT:	AUTHOR:	Curt Parfite, Team editor	DATE:	10/5/91	WORKING	READER	DATE	CONTEXT:
	PROJECT:	NOSC MicroCIM Program	REV:	10/9/91				
				10/26/91				
				12/4/91				
NOTES:		1 2 3 4 5 6 7 8 9 10						



NODE:	TITLE:	HYBRID APPLICATION REFERENCE MODEL EXPANDED DEPENDENTS OF HYBRID ASSEMBLY COMPONENTS	NUMBER:	VIEW 4-4
-------	--------	---	---------	----------

USED AT:	AUTHOR:	Curt Parks, Team editor	DATE:	11/18/91	CONTEXT:
	PROJECT:	NOSC MicroCIM Program	REV:	12/2/91	
	NOTES:	1 2 3 4 5 6 7 8 9 10			



NODE:	TITLE:	HYBRID APPLICATION REFERENCE MODEL EXPANDED PART MODEL	NUMBER:	VIEW 4-5
-------	--------	---	---------	----------

USED AT:	AUTHOR: Curt Parks, Team editor PROJECT: NOSC MicroCIM Program	DATE: 10/5/91 REV: 10/9/91 11/29/91 12/2/91 1/14/92	WORKING DRAFT	READER	DATE	CONTEXT:
NOTES: 1 2 3 4 5 6 7 8 9 10						

**ASSEMBLY CONSUMABLE (from 4-1)**

(Consumable Type)

**PROCESSING CONSUMABLE**

Process Cons Name (Solvent, Flux, Resist, etc.)

**PRODUCT CONSUMABLE**

Product Consumable Name (Wire, Epoxy, Paste, etc.)

**DEPOSITION COMPONENT (from 4-1)**

(Dep Component type)

**DEPOSITION RESISTOR**

Aspect Ratio  
Resistivity  
Resistor Geometry  
Resistor Min Width  
Resistor Min Length  
Resistor Max Aspect Ratio  
Resistor Overlap  
Resistor Shape  
Resistor Termination  
Sheet Resistivity  
Temp Coefficient of Resistivity  
Trim Path  
Volume Resistivity  
Pattern Value, Value Min & Max

**CONSUMABLE PROPERTY**

Cons Prop Name (Drying Time, Firing, Shelf Life, % Solids, Viscosity)  
  
Consumable Property Value

identifies material contained in

**WIREBOND (from 4-4)**

**DIELECTRIC**

Dielectric Loss Angle  
Dielectric Constant  
Dielectric Strength  
Dissipation  
Dissipation Factor

## 5. IGES APPLICATION INTERPRETED MODEL

The Application Interpreted Model (AIM) is an information model that describes the logical information structures required for accomplishing a physical implementation of an associated application reference model. The AIM is prepared at a level of abstraction that is sufficient for selecting the necessary IGES<sup>7</sup> entities for an application protocol.

The scope of this AIM is currently limited to LEP information contained in electronic computer-aided design (ECAD) design systems. These systems are in widespread use and translation between dissimilar systems is a high priority in the user community. IGES serves as the implementation for this information because most ECAD suppliers are familiar with the specification and support it in their software packages.

A broader scope for this AP that includes manufacturing, test, simulation, behavior and documentation is desired by users and manufacturers of LEPs. Much of this information is outside the scope (see also Abstract) of most ECAD systems and the IGES specification.

The graphical constructs of the AIM are presented in section 5.2 followed by the AIM diagrams in section 5.3. The AIM diagrams are divided into subsections as follows:

- |                        |  |
|------------------------|--|
| 5.3.1 Interface        | Interface object models are defined in this section. Each interface object model represents a "view" or "perspective" of an LEP in which one can exchange data. They describe the set of independent entities (DE Attribute - Subordination Status equals 0) that are in an IGES file which describe some aspect of an LEP. There are currently three interface objects; LEP Part Library IGES File, LEP Physical Layout IGES File and LEP Technical Illustration IGES File. Future interface objects might be LEP Schematic IGES File or LEP Manufacturing IGES File. |
| 5.3.2 LEP Specific     | This section defines objects that are unique and specific to LEPs.   |
| 5.3.3 Display Geometry | This section defines object that are common to any CAD/CAM system that utilizes 2-dimensional geometry.  |
| 5.3 4 Miscellaneous    | This section defines subordinate objects which when used in combination represent an LEP specific object.  |
| 5.3.5 DE Referenced    | This section defines objects that are only referenced from the DE section of another object.   |
| 5.3.6 DE Section       | This section defines value objects that represent pre-defined DE section values.   |

In order to conform to this AIM an ECAD system must be capable of reading and writing files that conform to the entire LEP Physical Layout IGES File interface model. It is appropriate to support all interface models, but it is not necessary in terms of conformance.

---

<sup>7</sup>. This section depends on the IGES document cited in section 2 for definitions and explanations of the format structure and the entities cited.

## 5.1 ARM to AIM Mapping

The ARM is an information model that documents the information structures of the subject application and provides the baseline from which candidate interpreted models are developed. For an IGES AP, the ARM is then used to develop the corresponding IGES Application Interpreted Model (AIM). The AIM shows how the information content from the ARM is to be expressed by a subset of IGES entities. Annotated outside the AIM object boxes are the ARM entities which provided the requirement. (Note: The reader should not infer a one-to-one mapping.)

The IGES entities selected for use in the AP specification should be selected to minimize the size of files. The options for the use of the entities within this subset must be restricted so that only one method is available for carrying each element of information from the ARM. The set of IGES entities and the necessary restrictions on the Global, Directory Entry, and Parameter Data Section field values are developed by using the ARM and the AIM.

## 5.2 IGES Structure and Syntax of the Application Interpreted Model

### 5.2.1 IGES File Structure

The following is the brief review of the IGES file structure from a predecessor<sup>8</sup> to this document:

“IGES provides format guidance for data transfer/archive. It defines several data structures or entities, whose pre-defined purpose may be geometry, annotation, or structure. The individual vendor can then map information contained in his proprietary database into this neutral format, then transfer that information to other vendor's applications, or archive the file for future use. IGES is fully three dimensional, and includes finite element, graphics, documentation/annotation, manufacturing and electrical entities.

The transfer medium is typically a nine-track magnetic tape. The transfer mode will commonly be character (ASCII) although binary is supported. The logical record length is 80 characters (block to 800 on tape) and is formatted for human readability and interaction. The advantage of the ASCII format are at the sacrifice of file size. However, there are standard file compression algorithms which may be used to achieve great reductions in file size, but the compressed files must be decompressed prior to translation. Also see ANSI X3.27-1978 labeled variable block.

The IGES data file structure consists of five sections. The start section, contains 72 columns of user comments which are not to be processed by the program other than listing to screen or printer. Next is the global section, a free format area specifying certain file attributes such as creation date, time, location, designer, units, display resolution, etc. The third section is the Directory Entry (DE) section containing fixed format attribute data (level, pen, translation, view, etc.) for each entity. The Parameter Data (PD) section follows and contains actual parameters for each of the entities in the DE section. Finally, the terminate section contains a single record containing the count of the records in each sec-

---

<sup>8</sup> L. O'Connell, ed., "Guide to the IGES Electrical Entities," unpublished, available from the IPO Office, Bldg 220, Rm A127, Gaithersburg, MD 20899, EACP-2.3 June 24, 1989; Appendix E.

tion. The entities come in two classes, those that are pre-defined and documented by the IGES committee (numbers 0001 to 5000), and those that are implementor definable (5001 to 9999). The constructs for a valid IGES file must conform to those specified in the current version of the IGES Specification.”

### 5.2.2 Global Values and Entities List

The following are IGES constructs that are used to fulfill the requirements of the AIM (View 4) for hybrid microelectronics technology. The IGES entities have been selected to ensure the constructs uniquely attributable to a hybrid product will be correctly transferred when they are post-processed. Other entities defined in the IGES Specification may be used for other purposes, however, these other entities should not be used for the purposes stated in the AIM. Parenthetical statements that follow the entities guide the reader to the relationships defined in the AIM. The IGES Specification should be consulted for the details of the syntactical constructs needed to produce valid IGES files.

**Globals:** (these are used to identify general product-file attributes)

<u>Global No.</u>	<u>Description</u>
3	Product identification from sending system
4	File name
5	System identification
12	Product identification for the receiving system
13	Model space scale
14	Unit flag
15	Units
21	Name of author
22	Author's organization
25	Date and time the model was created or last modified

#### IGES Entities used in the AIM:

The following categories for IGES documented entities are utilized within this AIM. Individual object definition models in the AIM contain usage restrictions (i.e., usage constraints) appropriate to the application. Please refer to the IGES document (version 5.1 or later) for detailed information regarding these entities. The Status field specifies the current status of the entity. Applicable values are;

Standard	The entity currently exists and does not need to be modified to be used within this AIM.
Gray	The entity currently exists and does not need to be modified to be used within this AIM. However, the entity is currently in the grey pages (approved, but untested) of the IGES document.
RFC	The entity is either new or it needs to be modified, however, an existing RFC which

describes the changes has already been submitted and is in the ballot process.

New The entity is new and an RFC needs to be submitted for it.

Modified The entity exists, but it must be modified in order to be used in this AIM.

<u>Status</u>	<u>Type</u>	<u>Form</u>	<u>Description</u>
Standard	100	0	Circular Arc
Standard	102	0	Composite Curve
Standard	104	1-3	Conic Arc
Standard	106	11	Copious Data - Planar Piecewise Linear Curve
Standard	106	63	Copious Data - Simple Closed Planar Curve
Standard	110	0	Line
Standard	112	0	Parametric Spline Curve
Standard	116	0	Point
Standard	124	0-1	Transformation Matrix
Modified	125	All	Predefined Planar Shape
Standard	126	0-5	Rational B-Spline Curve
Standard	132	0	Connect Point
Standard	212	0,1,6,7&8	General Note
Standard	308	0	Subfigure Definition
Standard	312	1	Text Display Template
Standard	314	0	Color Definition
Standard	320	0	Network Subfigure Definition
Modified	322	0-2	Attribute Table Definition
Standard	402	1	Group - Unordered With Back Pointers
Standard	402	14	Group - Ordered With Back Pointers
Modified	402	18	Flow Associativity
New	402	5xxx	Net Connection Associativity
Standard	406	1	Property - Definition Levels
Modified	406	2	Property - Region Restriction
Modified	406	5	Property - Line Widening
Standard	406	9	Property - Part Number
Standard	406	15	Property - Name
Standard	406	10	Property - Hierarchy
Modified	406	24	Property - Level to LEP Layer Map
Modified	406	26	Property - LEP Substrate Hole Property
Grey	406	27	Property - Generic Data
Modified	406	5xxx	Property - LEP Object Type/Sub-Type
New	406	5xxx	Property - Region Fill
New	406	5xxx	Property - LEP Component Placement Boundary
RFC	406	5xxx	Property - Definition Extents
New	406	5xxx	Property - LEP Fixed Component Placement

New	406	5xxx	Property - LEP Physical Layer Description
New	406	5xxx	Property - Instance Level Display
Standard	408	0	Subfigure Instance
RFC	408	1	Modified Subfigure Instance
Standard	420	0	Network Subfigure Instance
RFC	420	1	Modified Network Subfigure Instance
Standard	422	0-1	Attribute Table Instance
New	5xxx	0	Object Locator
New	5xxx	0	Planar Composite Area
New	5xxx	0	Electronic Component Definition
New	5xxx	0	Electronic Function Definition
RFC	5xxx	0	Modified Entities Definition

A some of the AIM entities are specific to a particular product type. These are listed below.

#### Hybrid Microcircuit Entities

Laser Trim Path  
 LEP Definition - Electrical Attributes  
 Package Symbol Definition - Electrical Attributes  
 Package Symbol Instance - Electrical Attributes  
 Wirebond

#### Printed Circuit Board Entities

Machined Hole  
 Machined Hole Figure Associativity  
 Machined Hole Figure Definition  
 Machined Hole Figure Instance

### **5.2.3 Basic Syntax used in the AIM**

A graphic notation has been adopted to describe the IGES data structures. The objective of these diagrams is the ease of developing unambiguous IGES translators and proof-reading files. The notation is not intended for use as a conceptual modeling language. The brief descriptions which follow explain the use of principal elements of the notation; the Object Definition Block, the Object Instance Block, the Object Value Block, and the Cardinality code.

#### **5.2.3.1 Object Definition Block**

The Object Definition Block is used to define an IGES entity type, form, directory entry values, parameter data values, and relationships to other IGES entities. There are several forms of the

Object Definition Block depending upon how the object is being used within the model.

Each Object must be defined at least once using the Object Definition Block.

The graphic in Figure 5-1 is used to define data, and relationships to other objects, for a particular object (usually a UoF). The graphic specifies the field name and required value(s)—if appropriate—for a particular field within the definition or instance of an object. This corresponds to the IGES Parameter Data Section. A Value Block can be referenced by either a Object Definition Block or a Object Instance block.

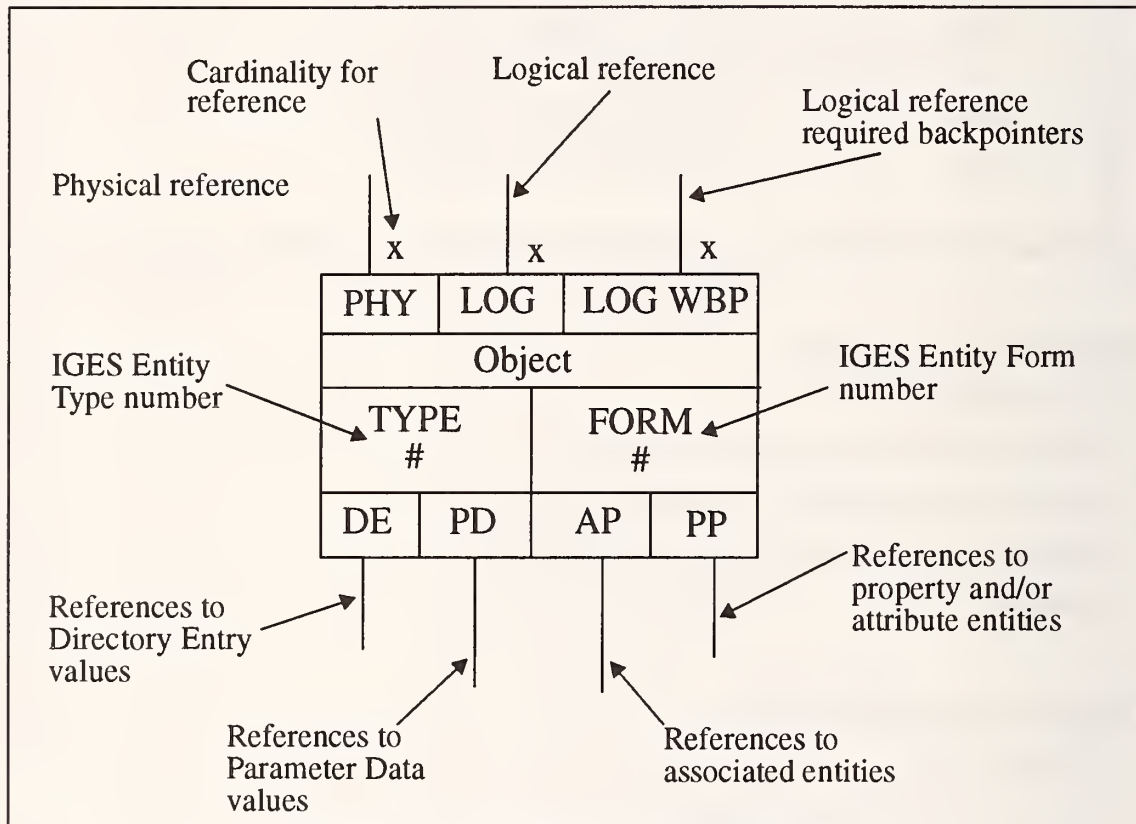


Figure 5-1. IGES Object and Referencing.

### 5.2.3.2 Object Instance Block

The graphic in Figure 5-2 defines a particular reference to a previously defined object. The long form is available if the particular instance needs to reference property, attributes, and/or associa-

tivity entities.

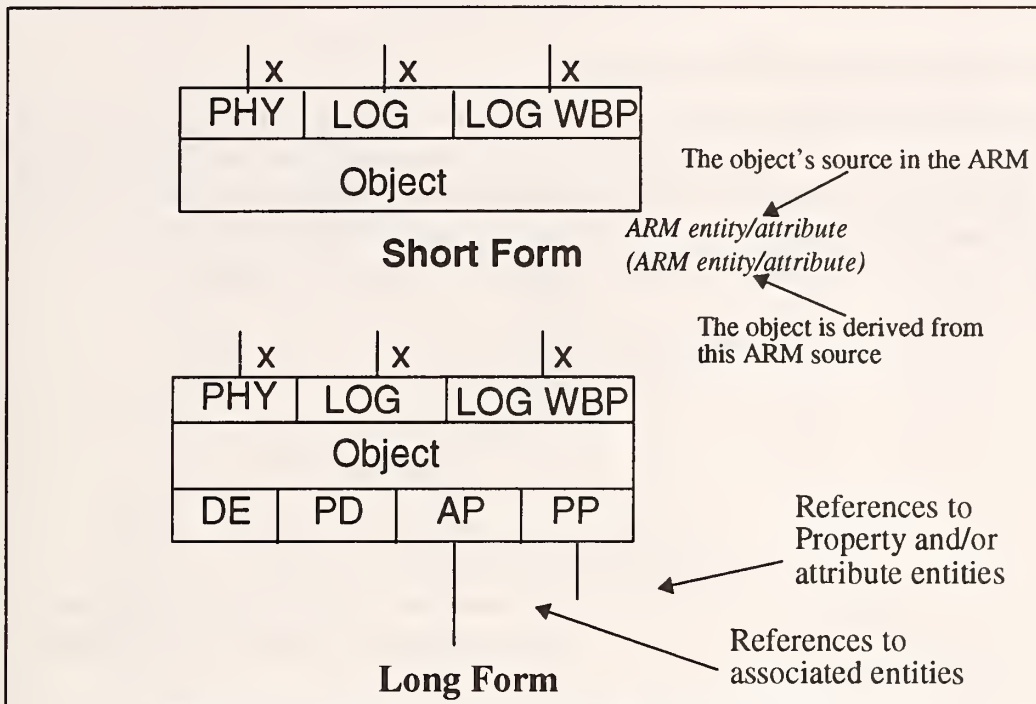


Figure 5-2. References to Previously Defined Object.

### 5.2.3.3 Object Value Block

The graphic in Figure 5-3 specifies the field name and required value(s), if appropriate, for a particular field within the definition or instance of an object. This corresponds to the IGES parameter data section.

The Value Definition Block is used to define a set of either directory entry values or parameter data values, which are used for a number of different objects.

A Value Block can be referenced by either a Object Definition Block or a Object Instance Block.

Value			
Index	Name	Value	
1	name1	Value	Field value is appropriate
2	name2	*	Any acceptable value
3	name3	⇒	Pointer to a predefined Instance Block
4	name4	value  ⇒	Value or pointer to a predefined Object Instance Block
5	name5	N/A	Value will be ignored
...	name...	...	

Figure 5-3. Object Field Value Restrictions.

### 5.2.3.4 Object Reference Mechanism

The Object Definition Block and Object Instance Block can both reference subordinate/child objects. Each object can reference a subordinate object through either the directory entry, parameter data, associativity backpointer or property pointer fields as shown in Figure 5-4. The subordinate objects can be referenced by either a physical, logical, or logical with backpointer, pointer mechanism. The representation cardinality indicators are shown in Figure 5-5.

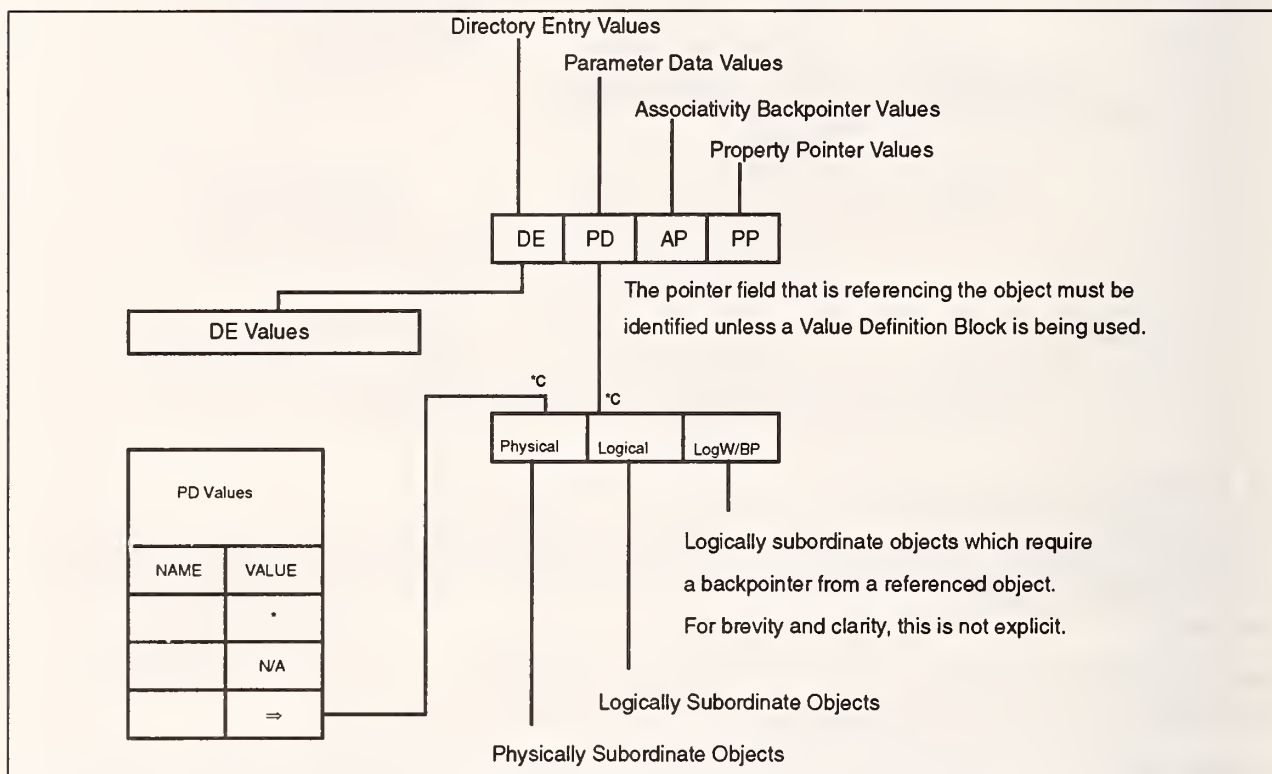


Figure 5-4. Reference Mechanism.

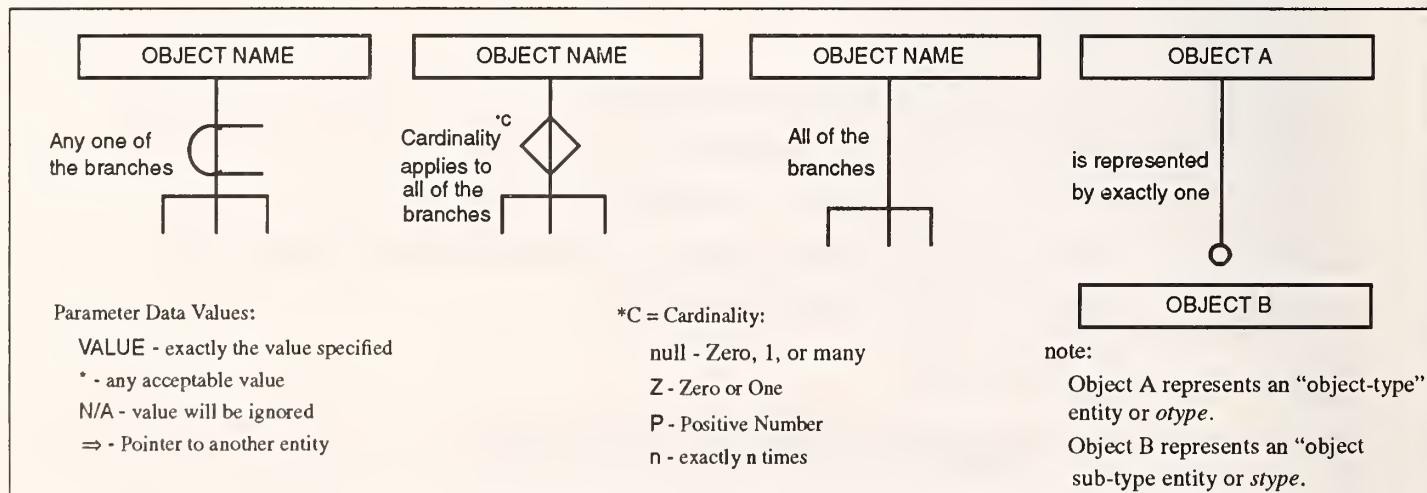


Figure 5-5. Representation Mechanism.

## 5.3 AIM Object Models

### 5.3.1 Interface Object Models

#### 5.3.1.1 LEP Part Library IGES File

##### Description:

The LEP Part Library IGES File object is an interface model, which enables you to exchange a library of LEP parts (i.e., Package Symbol Definitions, Padstack Definitions, Generic Part Definitions, etc.).

##### Requirements/Restrictions:

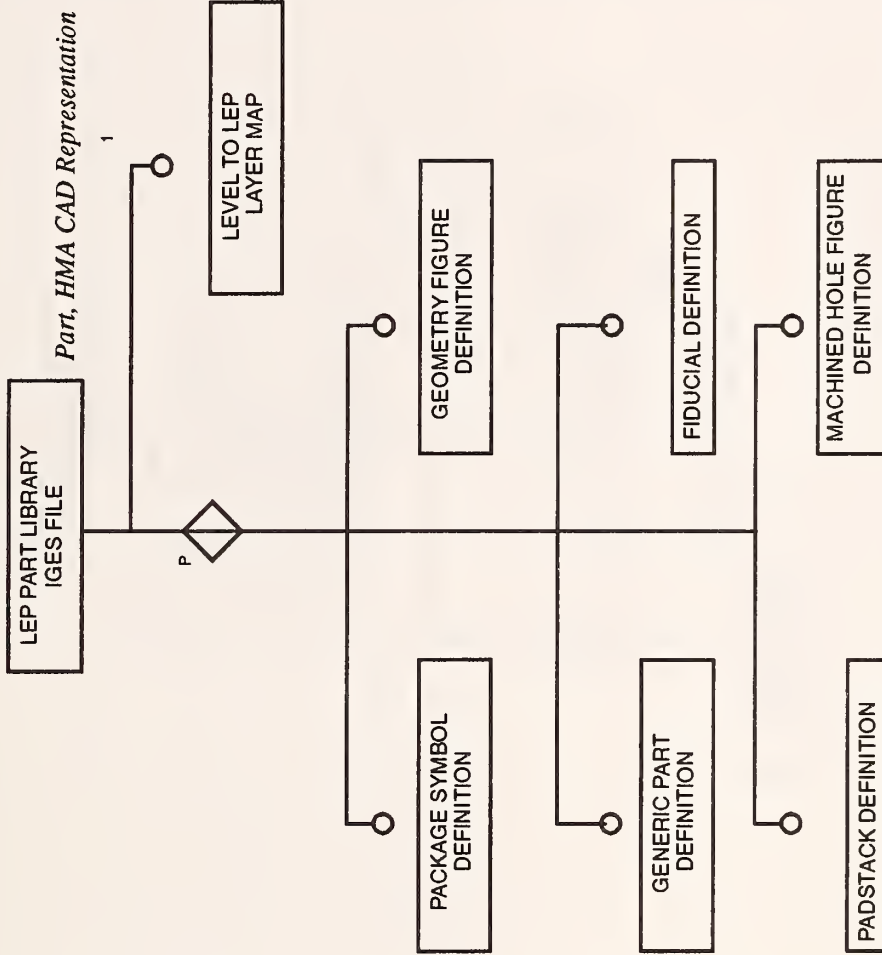
43

##### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.1.2 LEP Physical Layout IGES File

#### Description:

The LEP Physical Layout IGES File object is an interface model, which enables you to exchange LEP Physical Layout data. The IGES file may contain either an independent Panel Instance, Drawing Instance and/or LEP Instance.

#### Requirements/Restrictions:

A LEP Instance must appear in the file in at least one of the following locations:

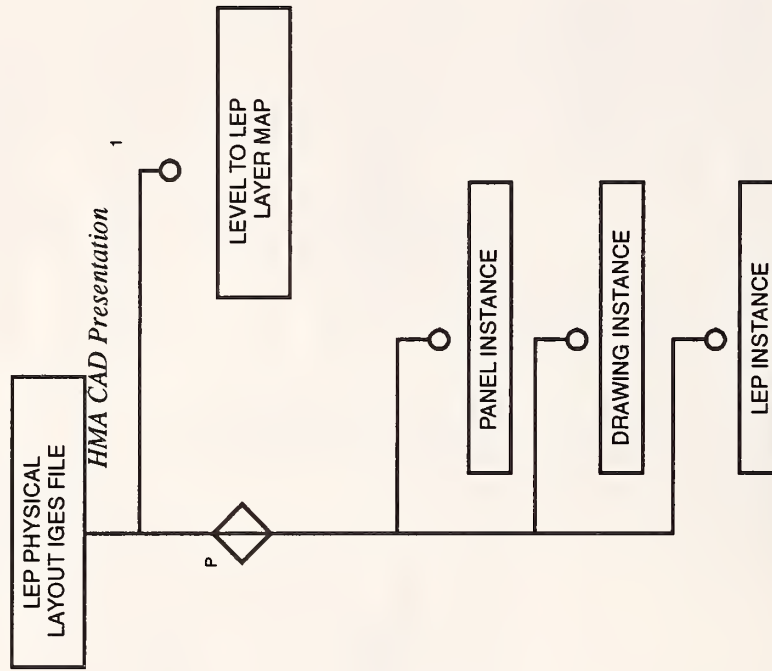
1. In the file as an independent entity
2. In a Drawing Definition
3. In a Panel Definition

#### Translation Usage Notes:

#### General:

#### Output:

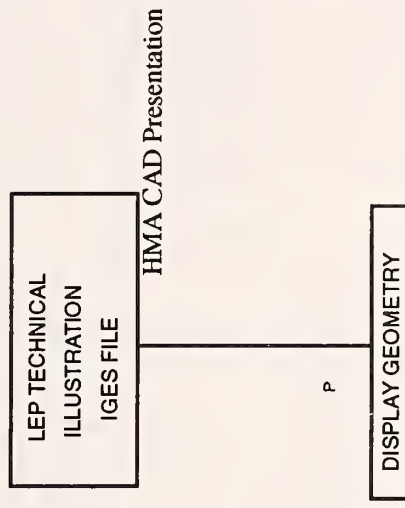
#### Input:

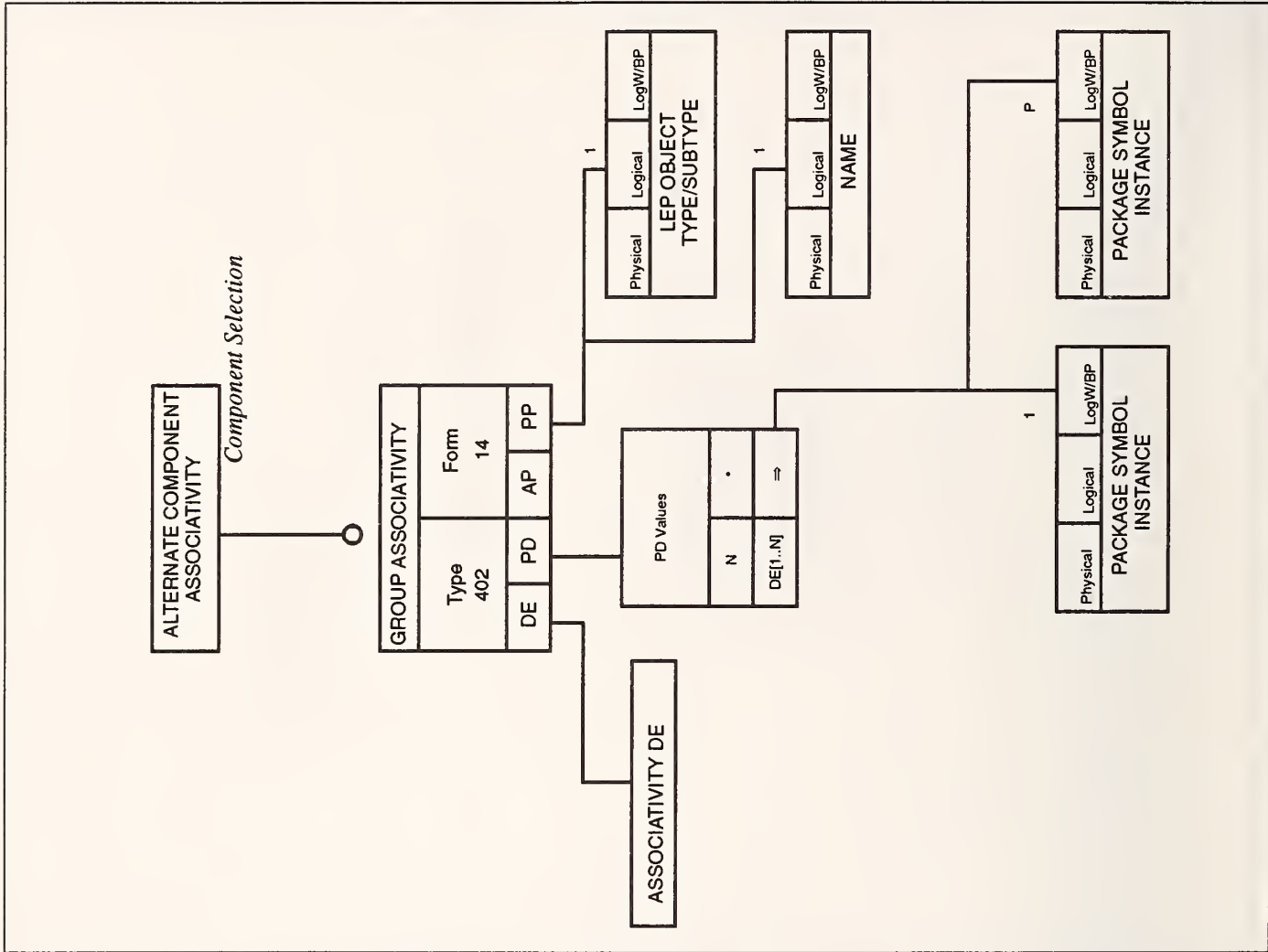


### 5.3.1.3 LEP Technical Illustration IGES File

**Description:**

The LEP Technical Illustration IGES File object is an interface model, which enables you to exchange a graphic representation of LEP data. There is no implied “intelligence” associated with this interface model.

**Requirements/Restrictions:****Translation Usage Notes:****General:****Output:****Input:**



## 5.3.2 LEP-Specific Object Models

### 5.3.2.1 Alternate Component Associativity

#### Description:

The Alternate Component Associativity object associates a single Package Symbol Instance with a set of alternate Package Symbol Instances. Any one of the alternate Package Symbol Instances can be used depending upon customer preference or manufacturing constraints.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*otype*=Alternate\_Component\_Associativity, *stype*=\*).
5. The first object referenced from the Group Associativity must be the Package Symbol Instance that is currently being used, followed by the alternate Package Symbol Instances.
6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

#### Translation Usage Notes:

#### General:

The reference designator of each component in the associativity must be the same.

### 5.3.2.2 Component Placement Associativity

#### Description:

The Component Placement Associativity object associates a group of Package Symbol Instances for the explicit purpose of being treated as a group with related placement restrictions. The Region Restriction property works in conjunction with the Component Placement Associativity.

#### Requirements/Restrictions:

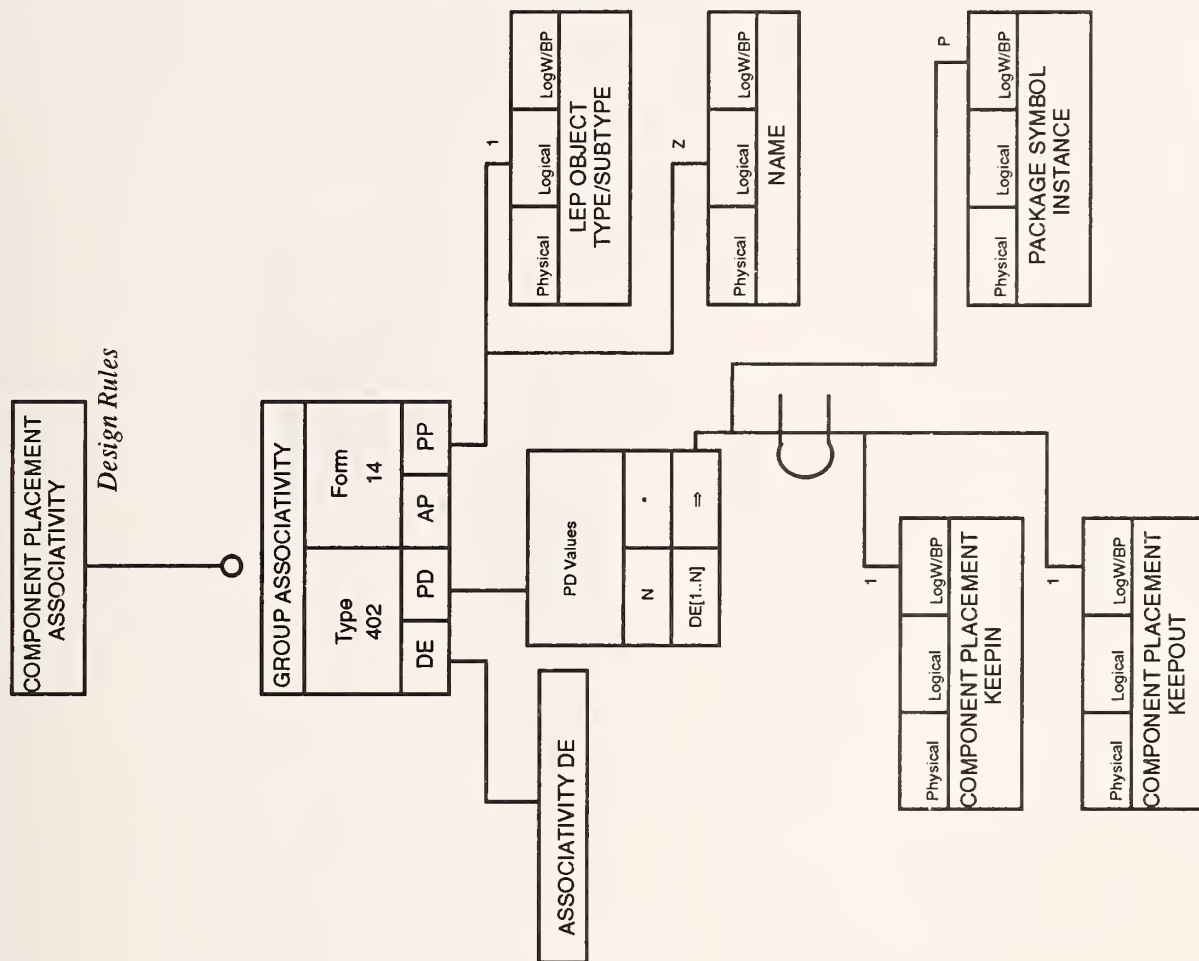
4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*otype*=Component\_Placement\_Associativity, *stype*=\*).
5. The first object referenced by the Component Placement Associativity must be either a Component Placement Keepin or a Component Placement Keepout, followed by the Package Symbol Instances which are affected by the Component Placement Associativity.
6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

#### Translation Usage Notes:

**General:**

**Output:**

**Input:**



### 5.3.2.3 Part (formerly Component) Placement Boundary

**Description:**

The Part Placement Boundary object is a closed curve, which represents the area on the LEP that a Package Symbol Definition encompasses. The Part Placement Boundary encompasses an XY area plus a lower and upper height for the area.

**Requirements/Restrictions:**

- 1. The curve must exist on the level defined for “component\_outline.”

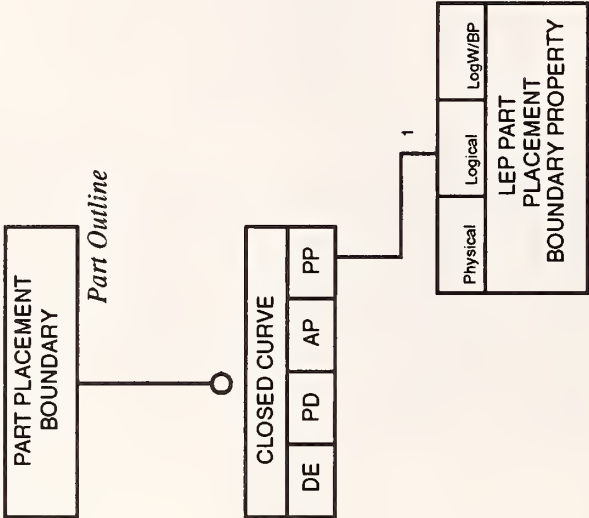
48

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.2.4 Component Placement Keepin

**Description:**

The Component Placement Keepin object is a closed curve, which represents an outline in which all Package Symbol Instances must be instantiated within.

**Requirements/Restrictions:**

You can only have one Component Placement Keepin per placement layer.

**Translation Usage Notes:**

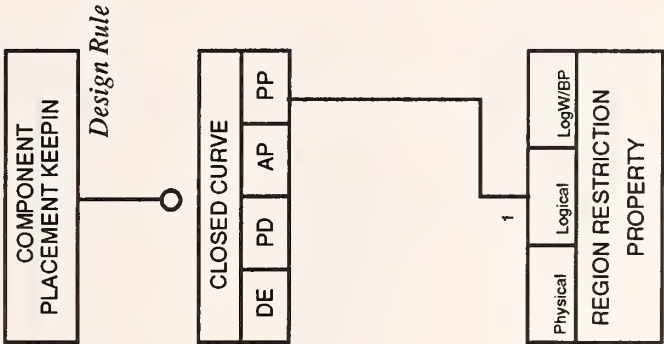
**General:**

The values for the Region Restriction Property should be as follows;

- VR=0
- CR=1
- TR=0
- RR=0

**Output:**

**Input:**



### 5.3.2.5 Component Placement Keepout

**Description:**

The Component Placement Keepout object is a closed curve, which represents an outline in which no Package Symbol Instances are allowed to be instantiated within.

**Requirements/Restrictions:**

**Translation Usage Notes:**

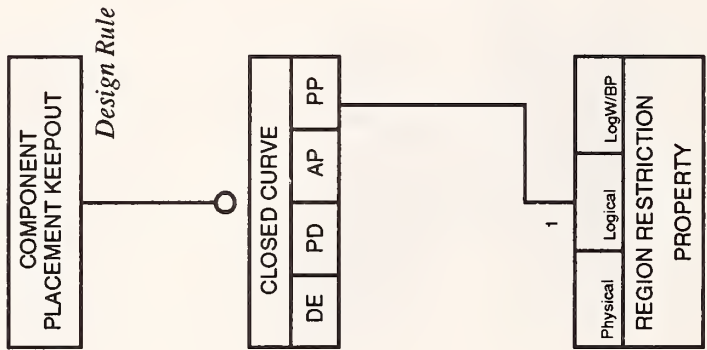
**General:**

The values for the Region Restriction Property should be as follows;

- VR=0
- CR=2
- TR=0
- RR=0

**Output:**

**Input:**



### 5.3.2.6 Part (formerly Component) Thermal Outline

#### Description:

The Part Thermal Outline object is a closed curve, which represents the area of the Package Symbol Instance that has thermal characteristics associated with it.

#### Requirements/Restrictions:

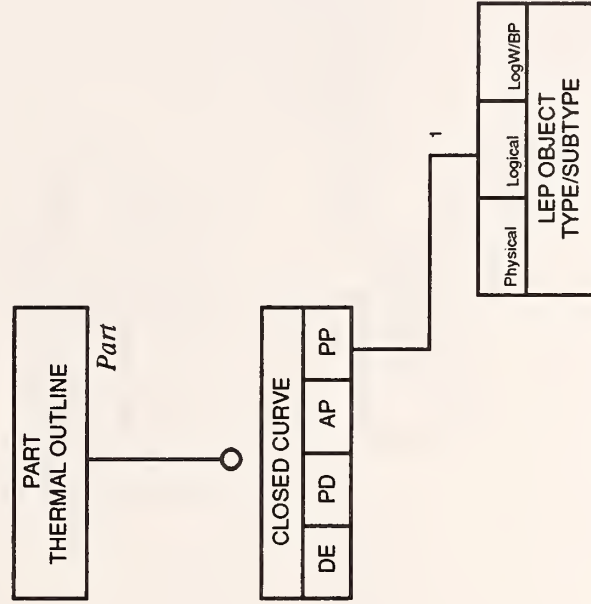
The LEP Object Type/Sub-Type property, which is referenced from the Closed Curve object entity, must specify (*otype*=Component\_Thermal\_Outline, *stype*=\*).

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



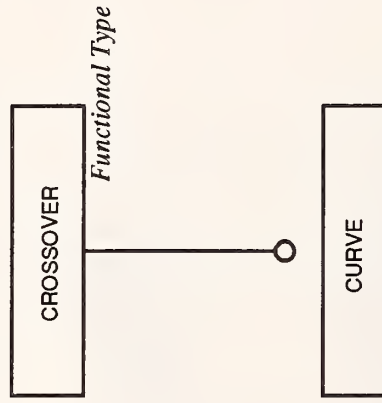
### 5.3.2.7 Crossover

**Description:**

The Crossover object is a linear path or closed area made of crossover dielectric material, which prevents electrical connectivity between two or more conductors.

**Requirements/Restrictions:****Translation Usage Notes:****General:**

- § 4. The Crossover geometry must exist on a level that is mapped to a physical dielectric crossover layer.

**Output:****Input:**

### 5.3.2.8 Decoupling Capacitor Associativity

#### Description:

The Decoupling Capacitor Associativity is an object that associates a specific decoupling capacitor with a Package Symbol Instance.

#### Requirements/Restrictions:

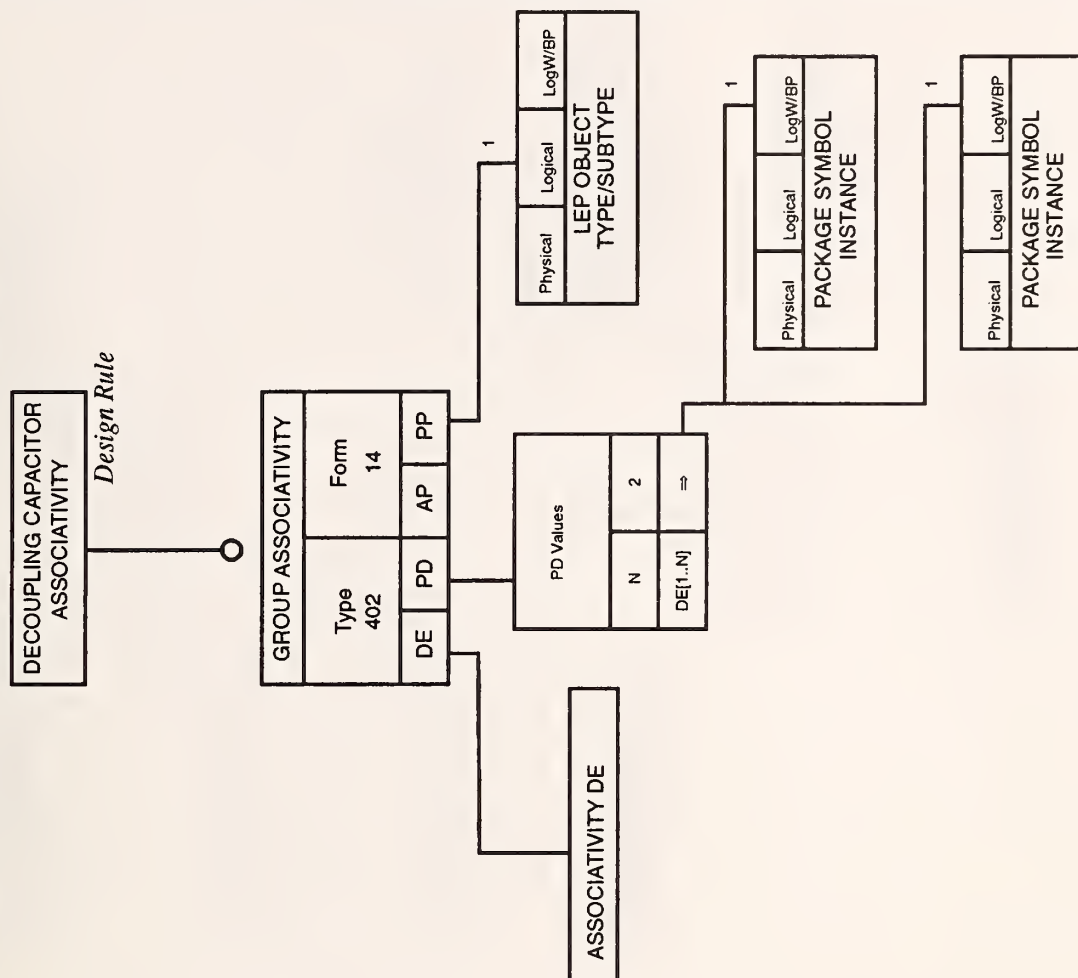
4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*otype*=Decoupling\_Capacitor\_Associativity, *stype*=\*).
5. The first object referenced from the Group Associativity must be the Package Symbol Instance representing a decoupling capacitor, followed by the Package Symbol Instance that requires the decoupling capacitor.
6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.2.9 Drawing Definition

#### Description:

The Drawing Definition object is a Subfigure Definition, which represents an engineering drawing of the LEP, a Panel or some portion of the LEP.

#### Requirements/Restrictions:

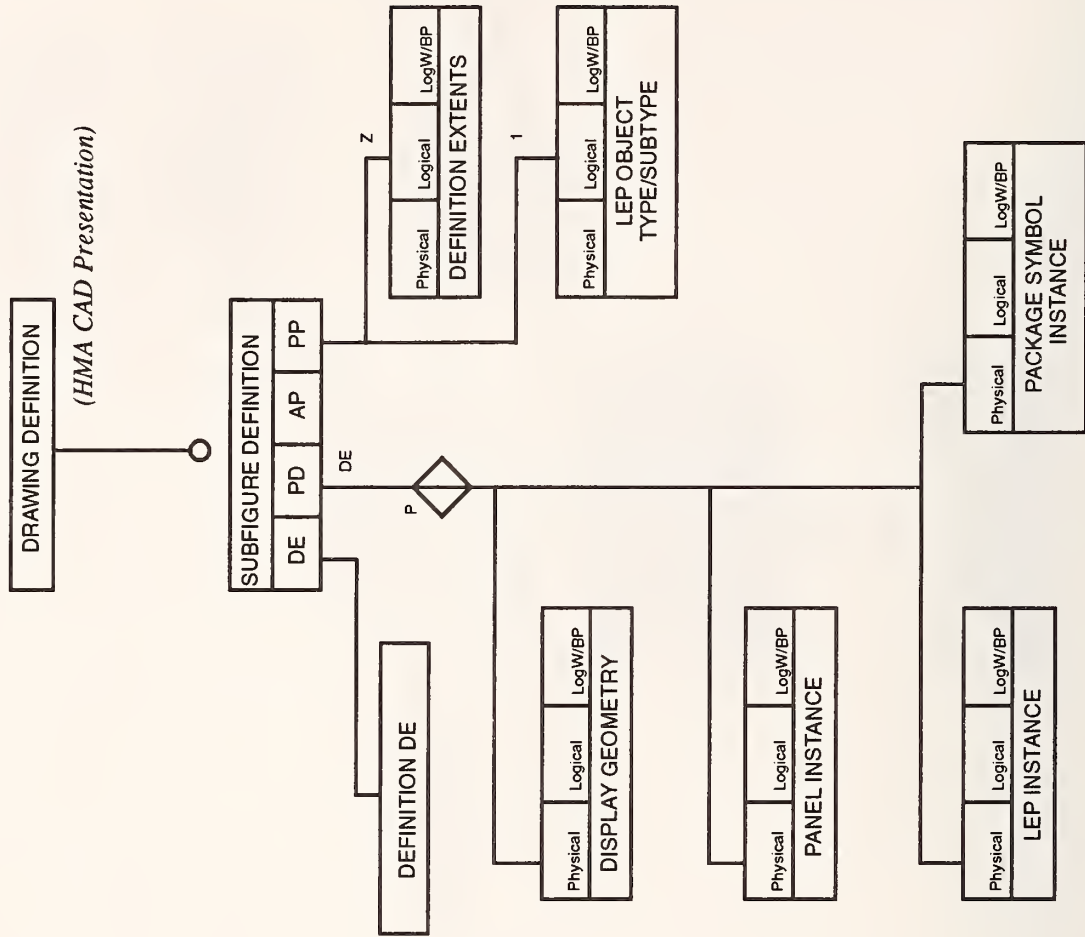
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype*=Drawing, *stype*=\*).
5. The NAME field in the Subfigure Definition must be unique (for all Drawing Definitions) within the scope of the IGES File.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.2.10 Drawing Instance

#### Description:

The Drawing Instance object is a instantiation of a Drawing Definition.

#### Requirements/Restrictions:

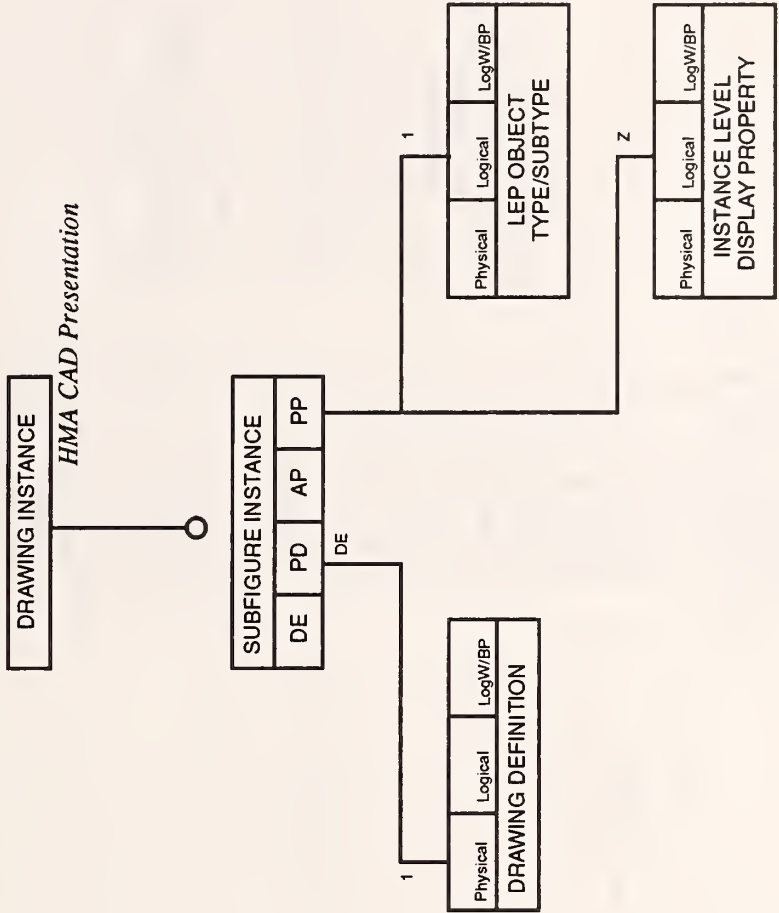
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (*otype*=Drawing, *stype*=\*).
5. The Drawing Instance can be implemented using either a Subfigure Instance or a Modified Subfigure Instance.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.2.11 Electronic Component Definition

#### Description:

The Electronic Component Definition object specifies the electronic characteristics of a particular component (i.e., pin swaps, gate swaps, device type, etc.).

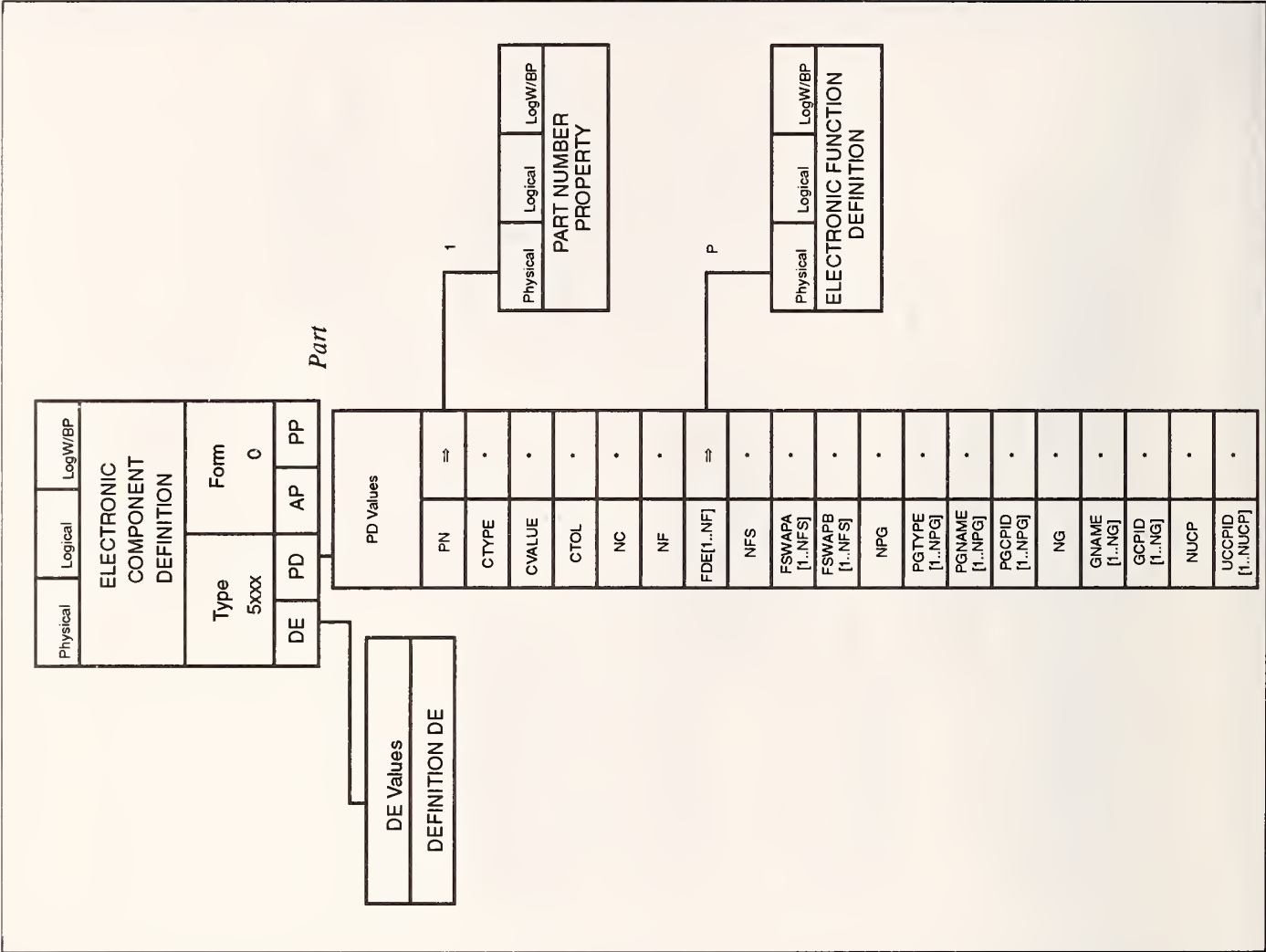
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.2.12 Electronic Function Definition

#### Description:

The Electronic Function Definition object specifies the electronic characteristics of a particular function (i.e., nand, nor, etc.) within an Electronic Component Definition.

#### Requirements/Restrictions:

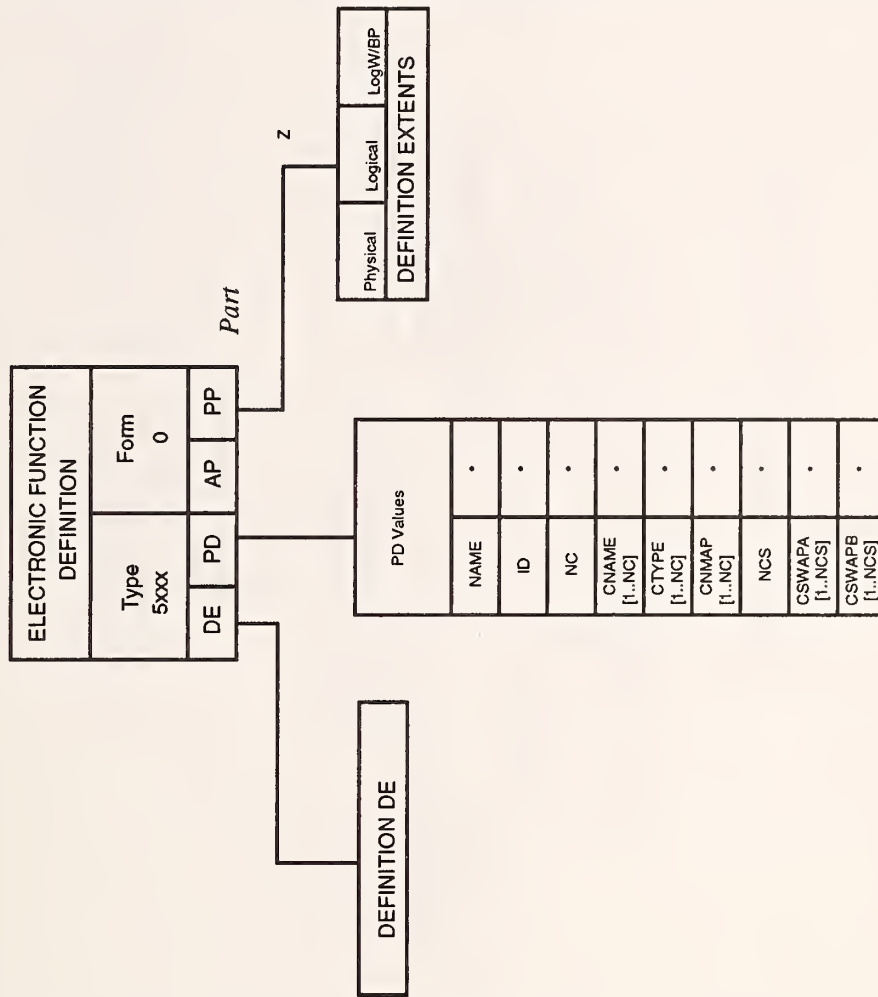
4. The CNAME field in the Electronic Function Definition must be unique within the scope of the Electronic Function Definition.

#### 57 Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.2.13 Fiducial Associativity

**Description:**

The Fiducial Associativity object associates a Package Symbol Instance and it's corresponding fiducial(s).

**Requirements/Restrictions:**

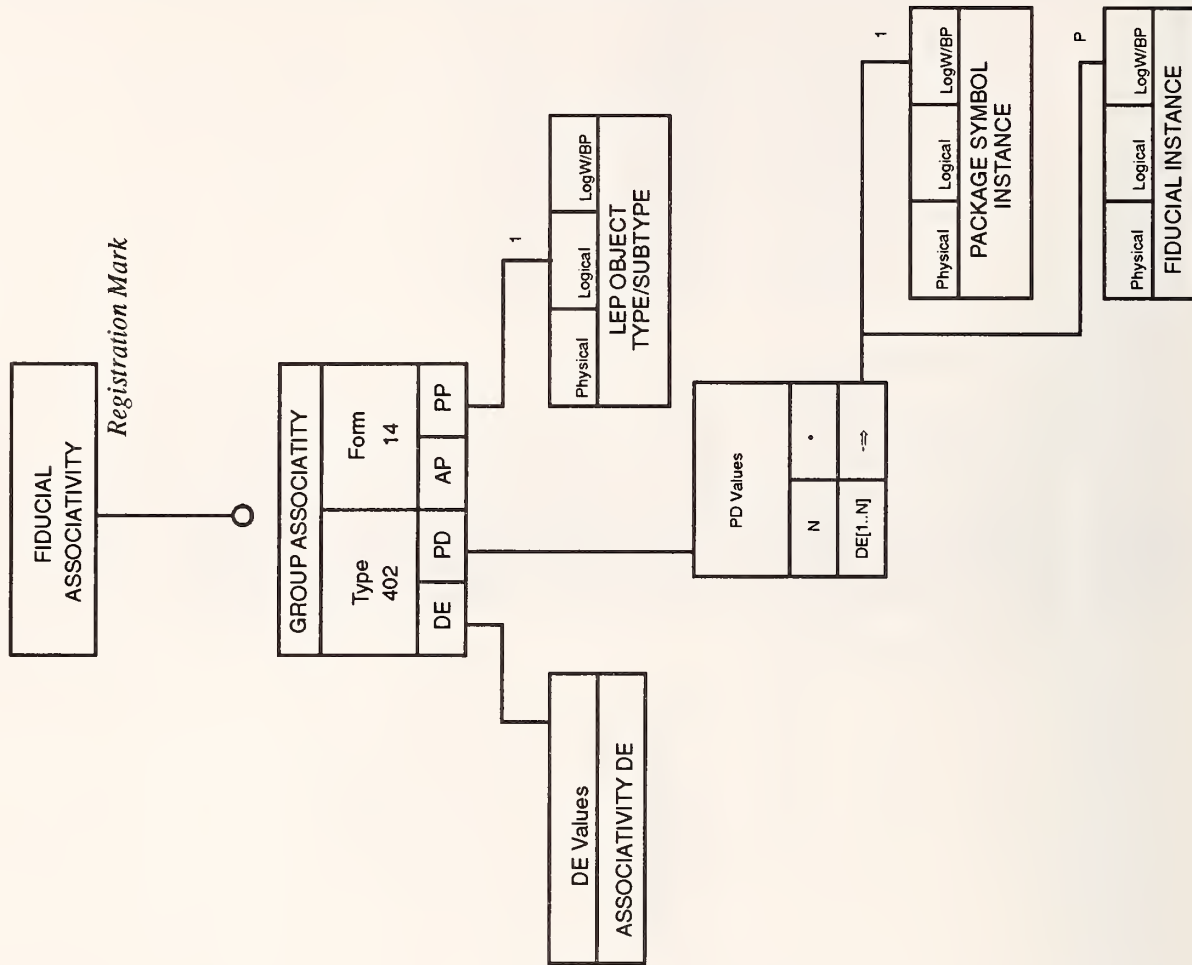
- 4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*otype*=Fiducial\_Associativity, *stype*=\*).
- 5. The first object referenced from the Group Associativity must be the Package Symbol Instance, followed by one or more Fiducial Instances.
- 6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



## 5.3.2.14 Fiducial Definition

### Description:

The Fiducial Definition object is a Subfigure Definition, which contains the display geometry objects that define a fiducial. A fiducial is a registration mark which enables vision assisted manufacturing equipment to properly align itself.

### Requirements/Restrictions:

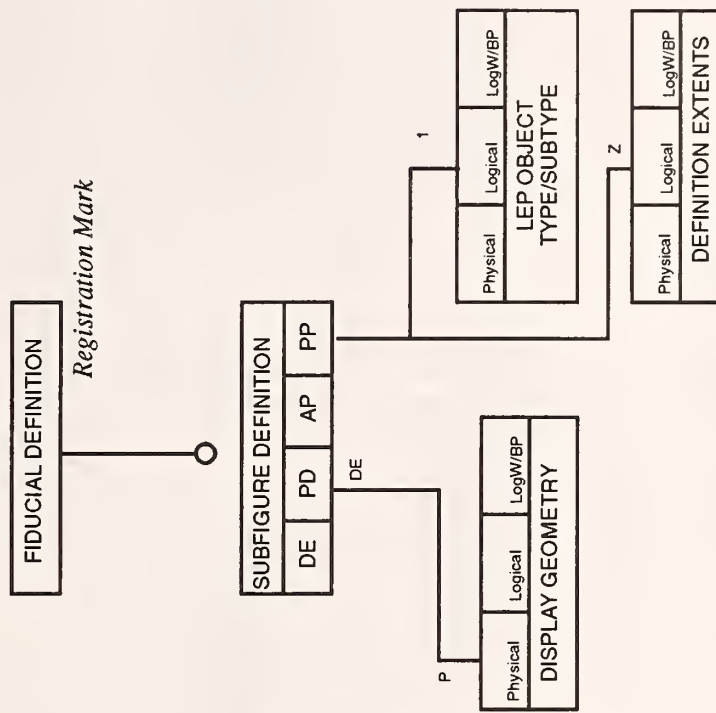
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype*=Fiducial, *stype*=\*).
5. The NAME field in the Subfigure Definition must be unique (for all Fiducial Definitions) within the scope of the IGES File.

### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.2.15 Fiducial Instance

#### Description:

The Fiducial Instance object is an instantiation of a Fiducial Definition.

#### Requirements/Restrictions:

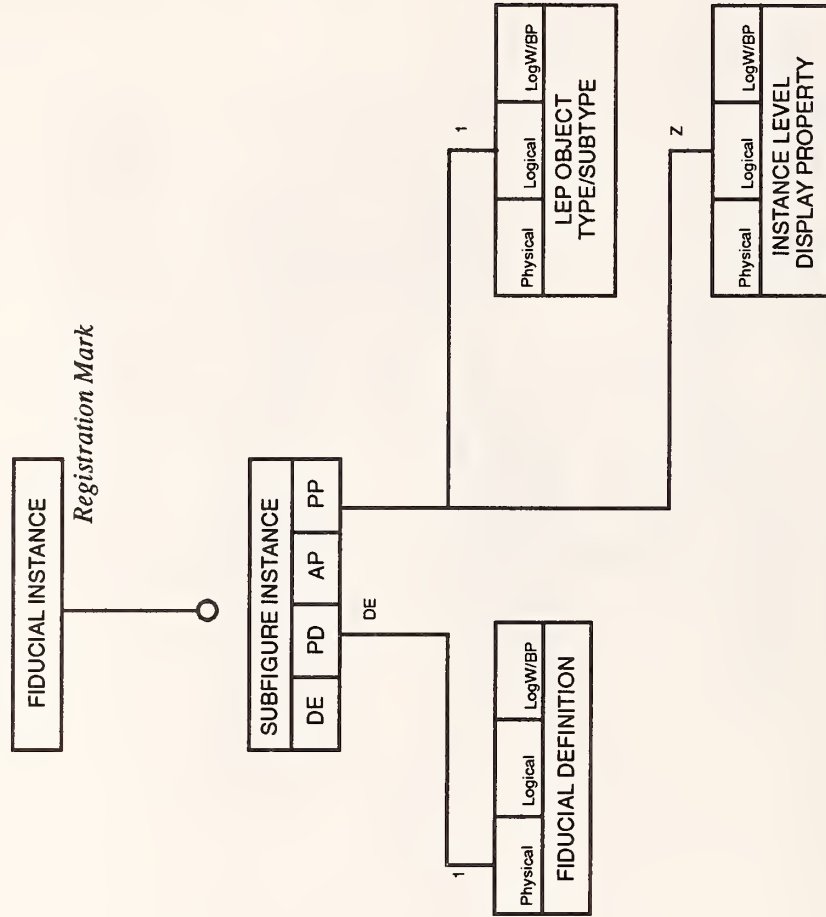
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (otype=Fiducial, stype=\*).
5. The Fiducial Instance can be implemented using either a Subfigure Instance or a Modified Subfigure Instance.

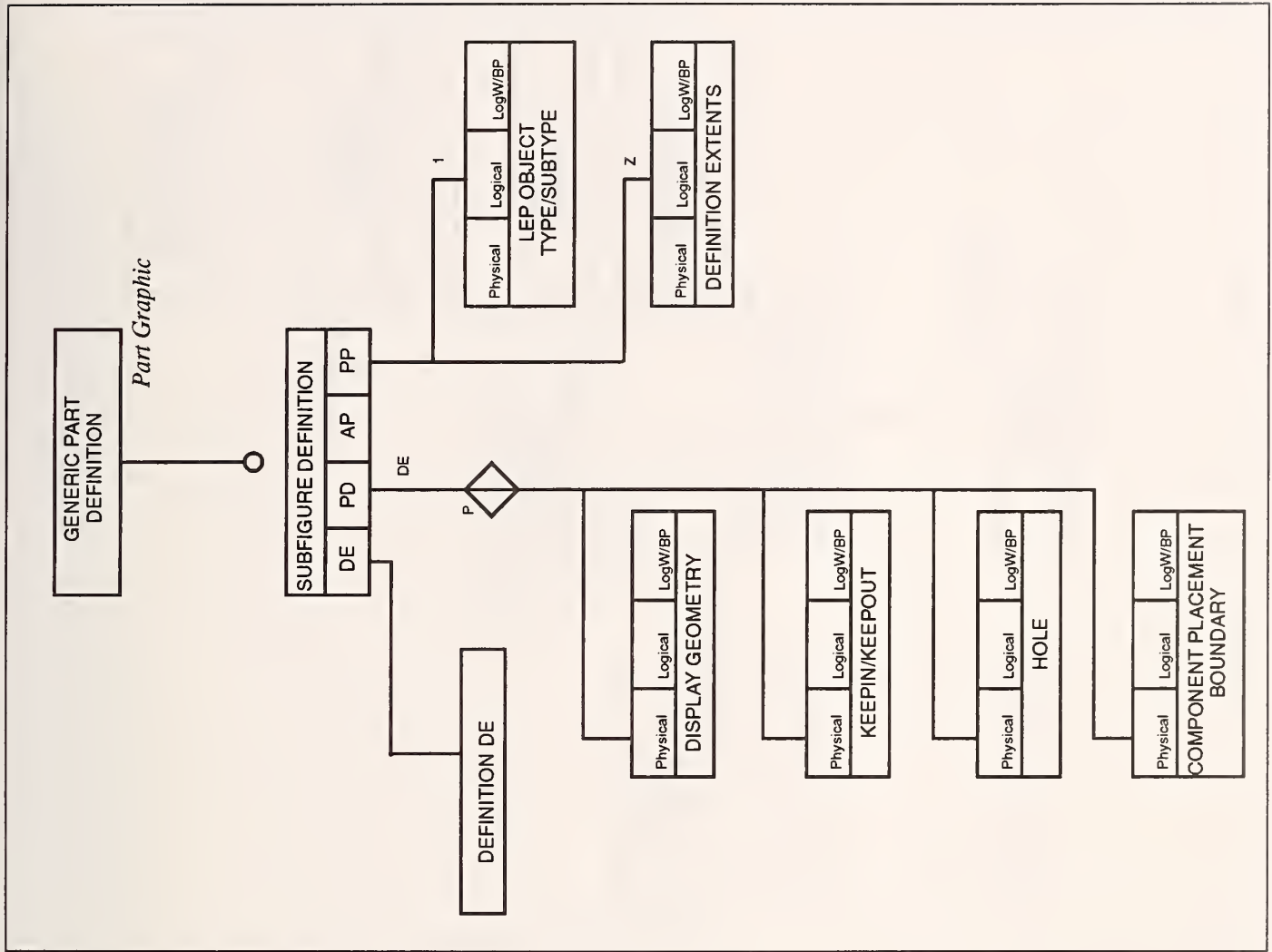
#### Translation Usage Notes:

##### General:

##### Output:

##### Input:





### 5.3.2.16 Generic Part Definition

#### Description:

The Generic Part Definition object is a Subfigure Definition, which specifies a set of constituent objects for the purpose of treating them like a fixed set or group.

#### Requirements/Restrictions:

4. A Routing Keepin or Placement Keepin cannot be subordinate to a Generic Part Definition.
5. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype*=Generic\_Part, *stype*=\*).
6. The NAME field in the Subfigure Definition must be unique (for all Generic Part Definitions) within the scope of the IGES File.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:

### 5.3.2.17 Generic Part Instance

#### Description:

The Generic Part Instance object is an instantiation of a Generic Part Definition.

#### Requirements/Restrictions:

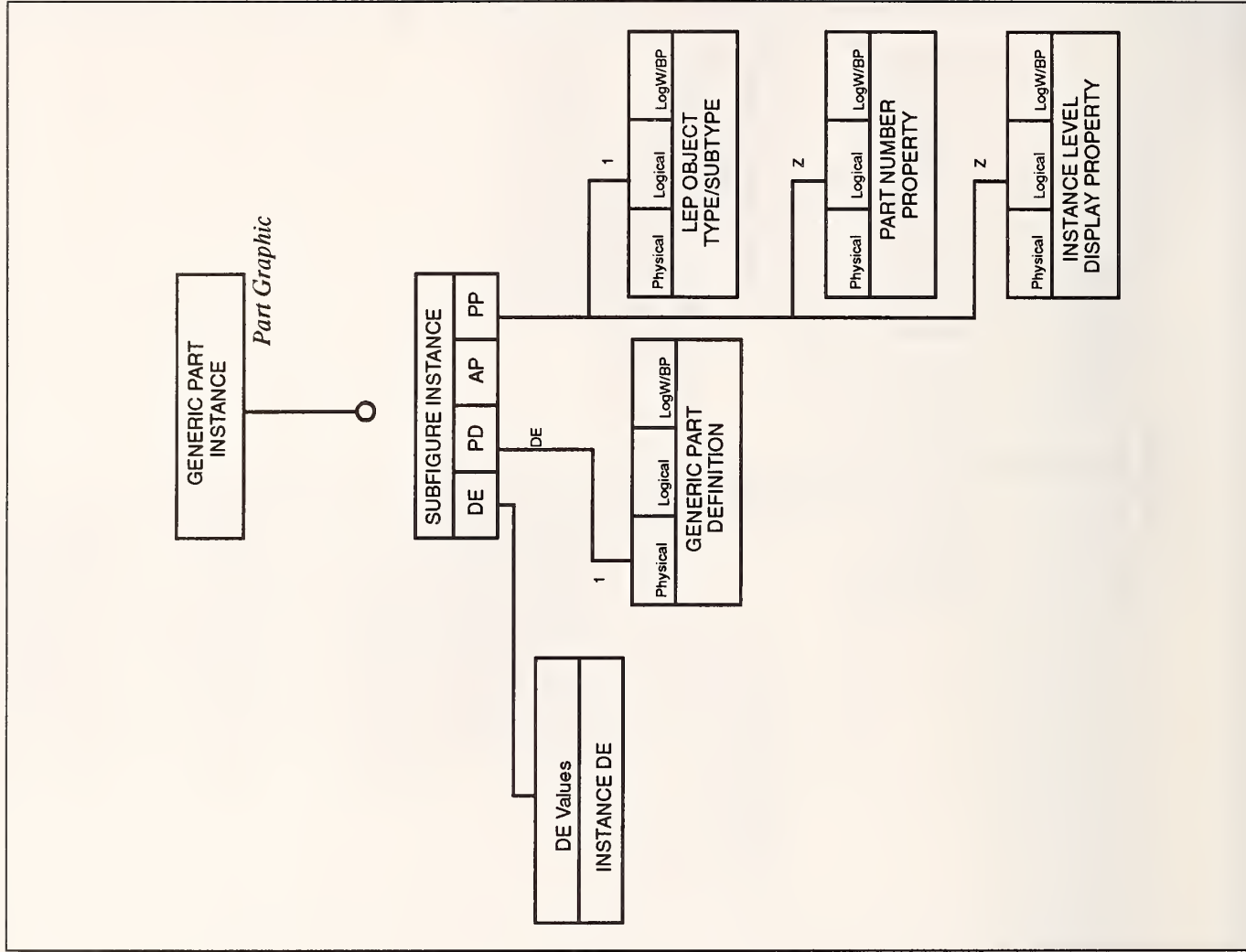
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (*otype*=Generic\_Part, *stype*=\*).
5. The Generic Part Instance can be implemented using either a Subfigure Instance or a Modified Subfigure Instance.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



# 5.3.2.18 Hole

## Description:

The Hole object specifies the location of a hole in one or more layers of the LEP. The hole can be any shape and can be manufactured in a variety of ways (i.e., drilled, punched, milled, burned, etc.).

## Requirements/Restrictions:

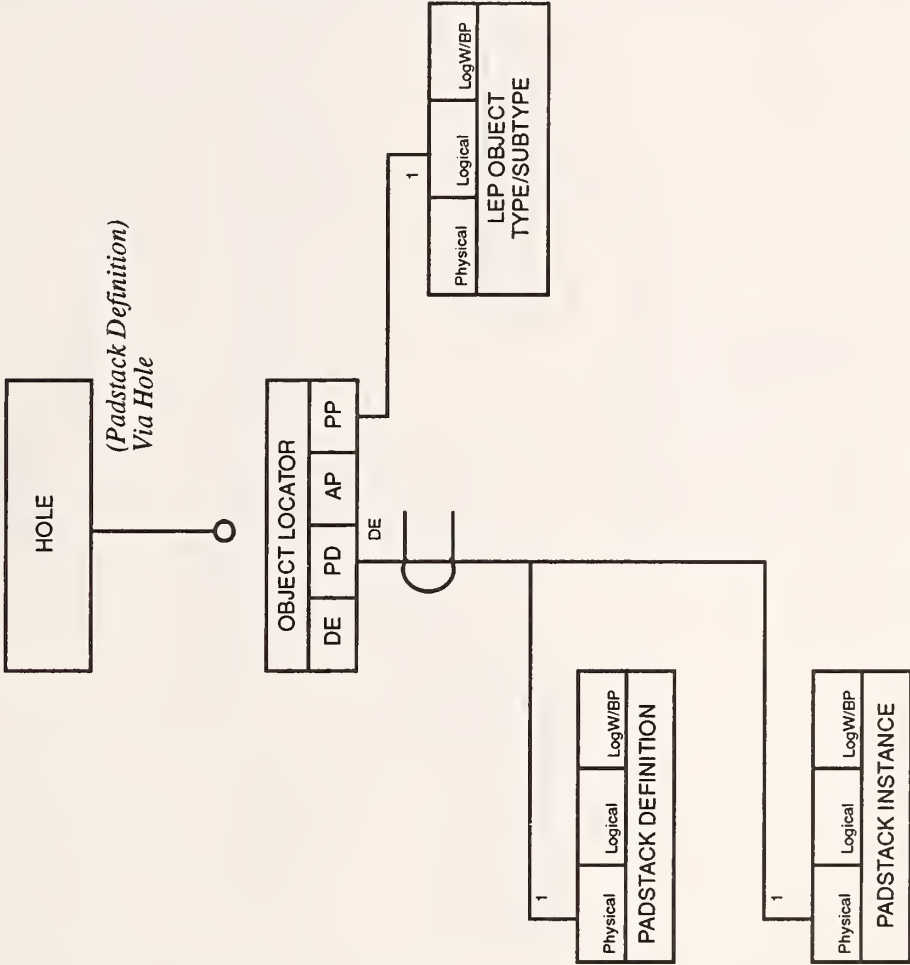
- 4. If the Hole is subordinate to a definition that is intended to be instantiated on the LEP (i.e. Package Symbol Definition), it should reference a Padstack Definition. If the Hole is subordinate to a LEP Definition, it should reference a Padstack Instance.
- 5. The LEP Object Type/Sub-Type property, which is referenced from the Object Locator object, must specify (*otype*=Hole, *stype*=\*).

## Translation Usage Notes:

**General:**

**Output:**

**Input:**



### 5.3.2.19 Join

#### Description:

The Join object represents any physical conductive material (i.e., conductive filled area, conductive path, or via) that is electrically common within a Net.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from each Join object must be specified as follows:

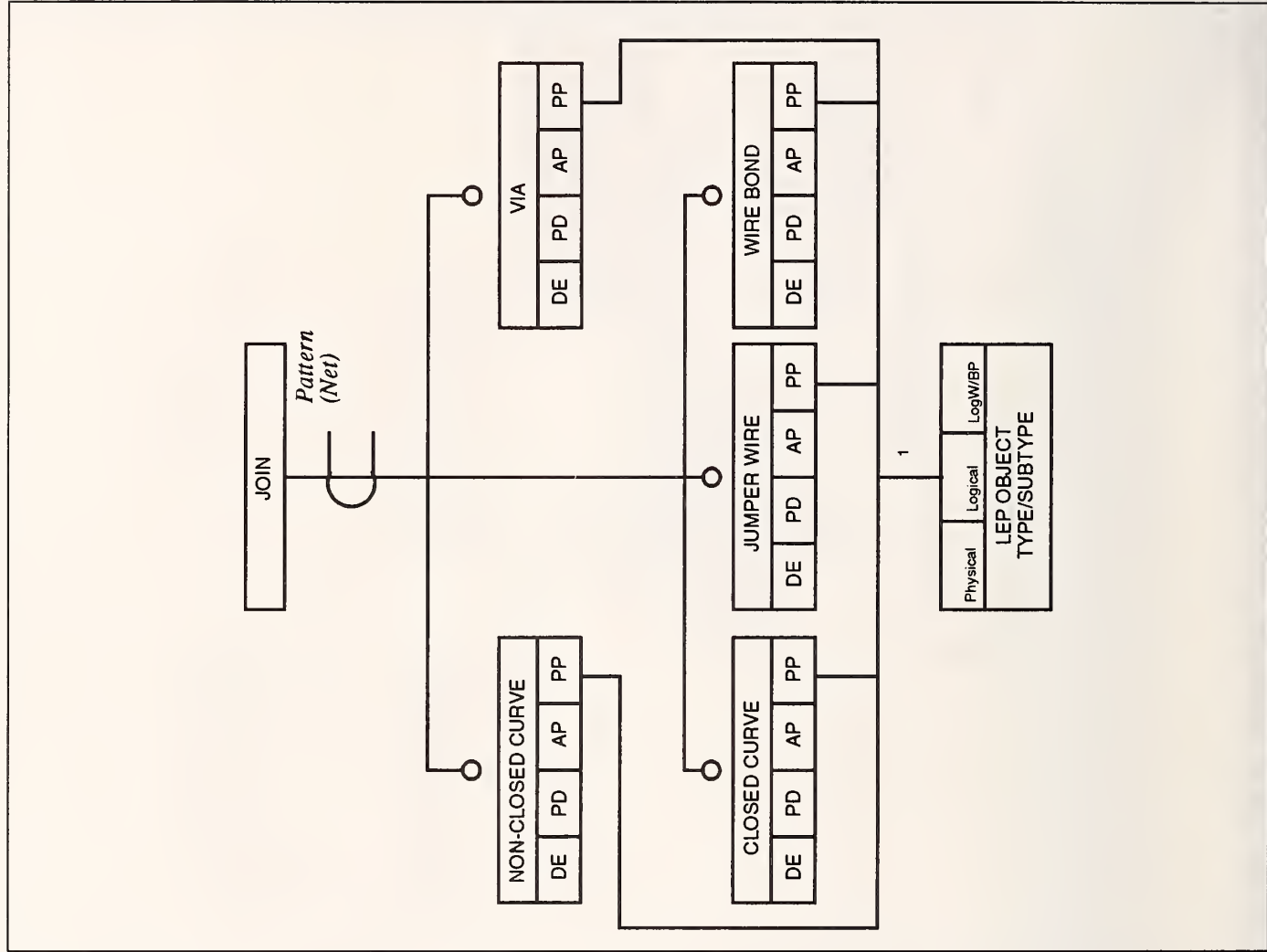
Non-Closed Curve	otype=Join	stype=Path
Closed Curve	otype=Join	stype=Area
Jumper Wire	otype=Join	stype=Jumper Wire
Via	otype=Join	stype=Via
Wire Bond	otype=Join	stype=Wire Bond

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.2.20 Jumper Wire

**Description:**

The Jumper Wire object is a conductive wire that is used to “jump” across one or more conductive paths. It is typically used to join two separate substrate nets into one design net.

**Requirements/Restrictions:**

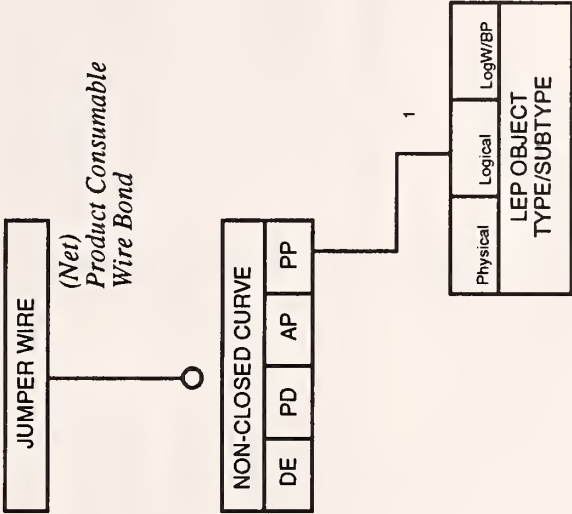
- 4. The LEP Object Type/Sub-Type property, which is referenced from the Non-Closed Curve object, must specify (*otype*=Join, *stype*=Jumper\_Wire).

 **Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.2.21 Keepin/Keepout

**Description:**

The Keepin/Keepout object is any one of the specific keepin or keepout region restrictions.

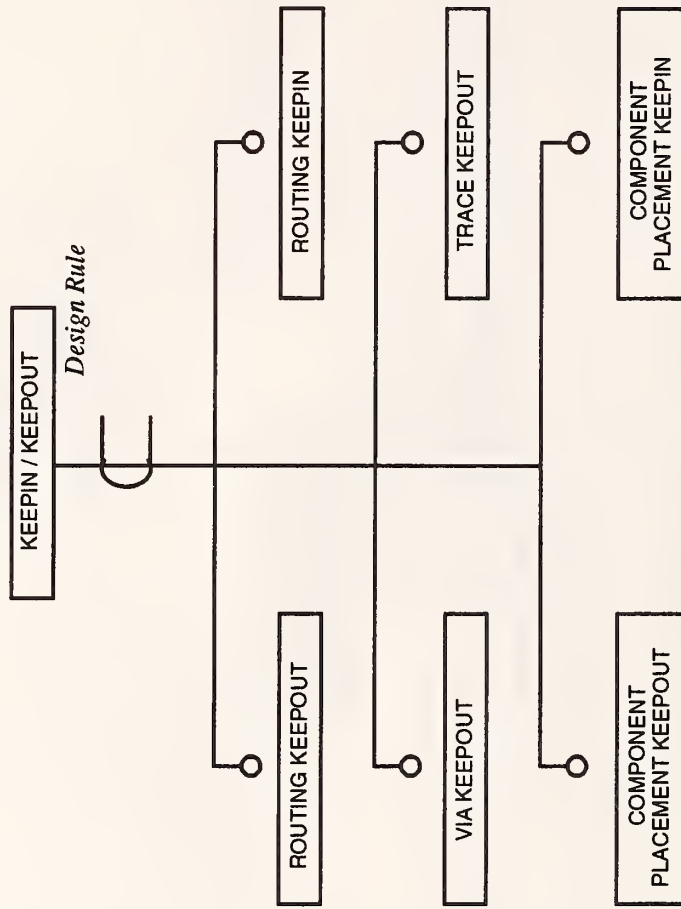
**Requirements/Restrictions:**

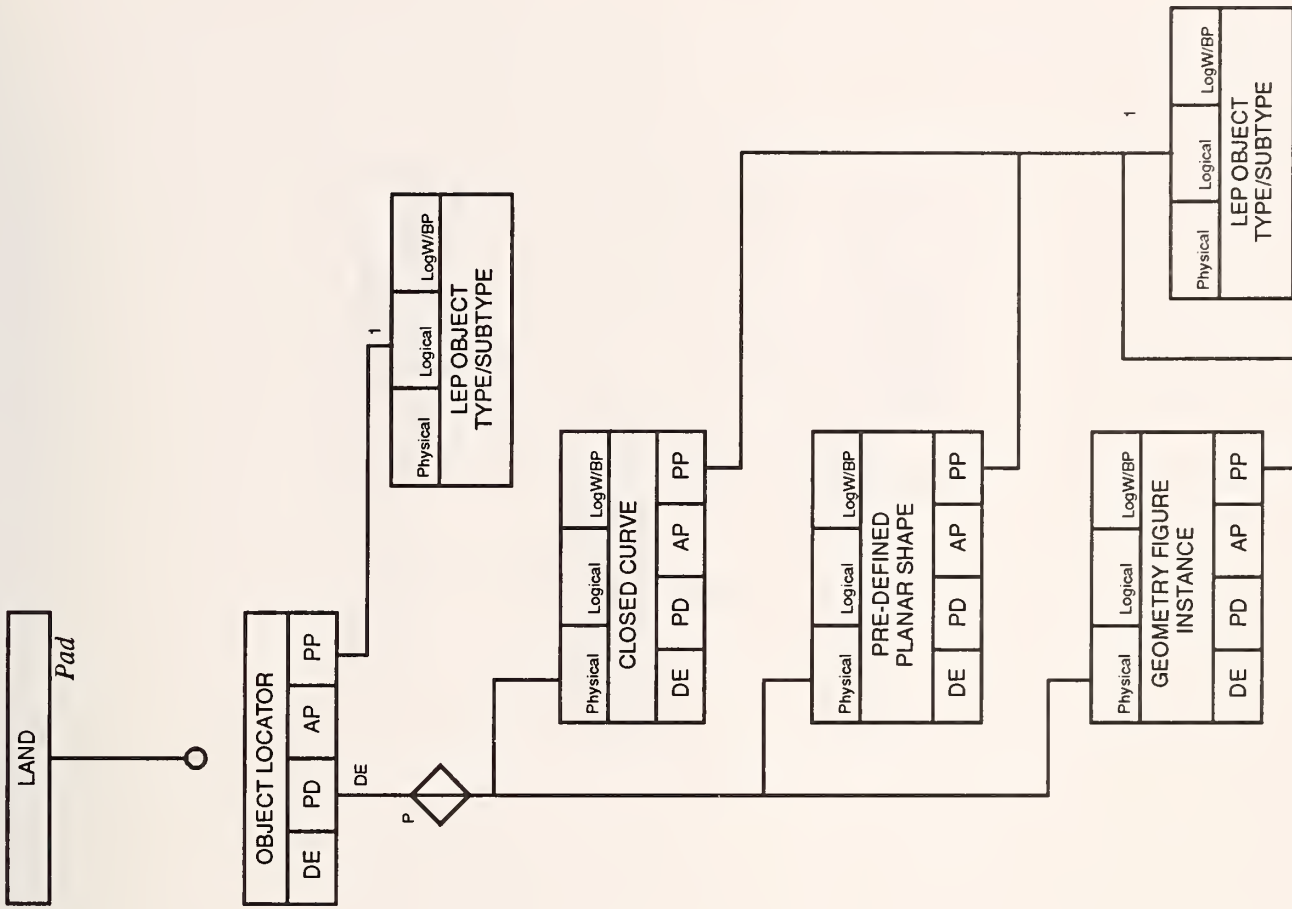
**Translation Usage Notes:**

**General:**

**Output:**

**Input:**





### 5.3.2.22 Land

#### Description:

The Land object specifies the geometry of a conductive pattern which is used for electrical connection or package symbol attachment.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Object Locator must specify (*otype*=Land, *stype*=Group)
5. The LEP Object Type/Sub-Type property, which is referenced from the Closed Curve, Pre-Defined Planar Shape, and Geometry Figure Instance, must specify (*otype*=Land, *stype*=Anti | Regular | Thermal).

#### Translation Usage Notes:

#### General:

When a Land object (*otype*=Land, *stype*=Group) is subordinate to a Padstack Definition, you can have land geometry for each possible object type/sub-type (anti, regular and thermal). When a Land object (*otype*=Land, *stype*=Group) is subordinate to a Padstack Instance, you can have only one land geometry (anti, regular or thermal). You can only have one Land object (*otype*=Land, *stype*=Group) for each LEP functional layer that the padstack encompasses.

### 5.3.2.23 Laser Trim Path

**Description:**

The Laser Trim Path object defines the path of a trim channel on a deposition type package symbol (i.e., screened resistor). The Laser Trim Path can be either static (passive) or dynamic (active).

**Requirements/Restrictions:**

- 4. The LEP Object Type/Sub-Type property, which is referenced from the Non-Closed Curve object, must specify (*otype=Laser\_Trim\_Path, stype=\**).

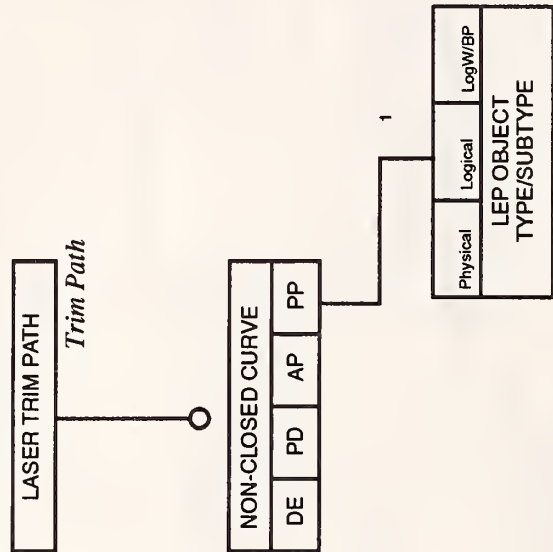
**Translation Usage Notes:**

**General:**

The width of the trim channel is defined by the DE Line Weight attribute value of the entity being used to represent the Laser Trim Path.

**Output:**

**Input:**



### 5.3.2.24 Layer Outline

#### Description:

The Layer Outline object defines the outline (boundary) for a specific physical layer of the LEP (i.e., substrate, power plane, etc.).

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Closed Curve object, must specify (*otype*=Layer\_Outline, *stype*=\*).

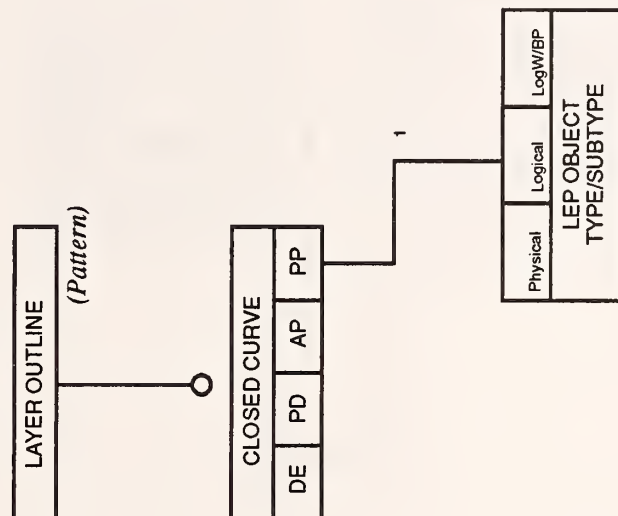
#### Translation Usage Notes:

#### General:

Only one Layer Outline can exist for each LEP Physical Layer.

#### Output:

#### Input:



### 5.3.2.25 LEP Artwork Stackup Property

**Description:**

The LEP Artwork Stackup Property object maps directly to the IGES PWB Artwork Stackup Property (Type 406 Form 25). Please refer to the IGES specification for additional information.

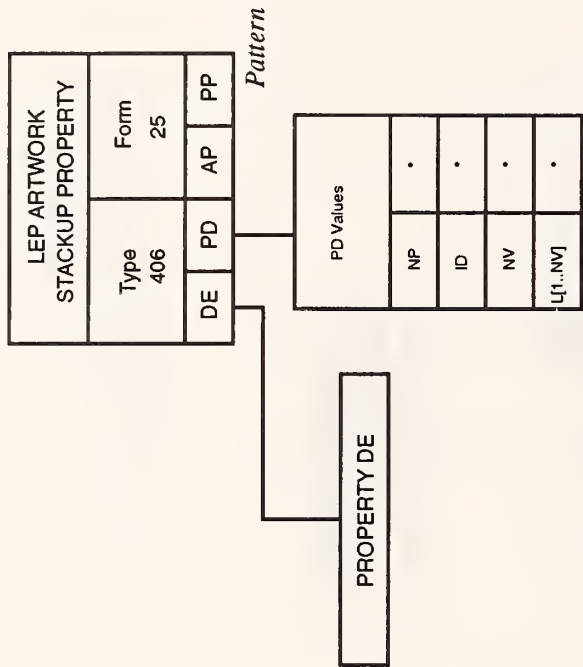
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



5.3.2.26 LEP Part (formerly Component) Placement Boundary Property

Description:

The LEP Part Placement Boundary Property object maps directly to the IGES LEP Part Placement Boundary Property (Type 406 Form 5xxx). Please refer to the IGES specification for additional information.

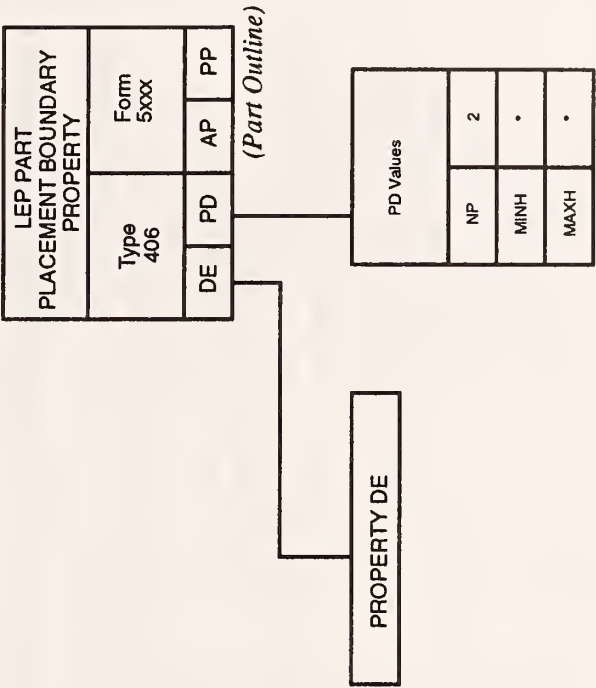
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.2.27 LEP Definition

#### Description:

The LEP Definition object is a Network Subfigure Definition, which specifies all of the constituent objects that are required to define the LEP.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Network Subfigure Definition object, must specify (*otype*=Layered\_Electrical\_Product, *stype*=\*).
5. The NAME field in the Network Subfigure Definition must be unique (for all LEP Definitions) within the scope of the IGES File.
6. There are no Connect Point Entities referenced from the LEP Definition. This implies that you cannot represent "true" hierarchy. The Network Subfigure Definition is used instead of a Subfigure Definition to allow for the eventual representation of hierarchy.
7. The following Attribute Table objects can be referenced from the LEP Definition:

#### Electrical Attribute List

6001	Component Placement Grid
6002	Pin Placement Grid
6003	Via Placement Grid
6004	Conductor Path and Area Grid
6005	Default Padstack Size
6006	Component to Component Placement Clearance
6007	Padstack to Padstack Placement Clearance
6008	Conductor to Conductor Placement Clearance

6009	Conductor to Padstack Placement Clearance
6010	Dielectric to Padstack Clearance
6011	Dielectric to Deposition Component Clearance
6012	Dielectric to Conductor Overlap
6013	Component Placement Orientation Rule
6014	Routing Orientation Rule
6015	Padstack No Connect Rule
6016	Via Under Padstack Rule
6017	Net Length Rule
6024	Generic Design Rule
6026	Hybrid Resistor Length Step Size
6027	Hybrid Resistor Minimum Dimension
6028	Hybrid Resistor Maximum Dimension
6029	Hybrid Resistor Minimum Allowed Area
6030	Hybrid Resistor Maximum Allowed Area
6031	Hybrid Resistor Minimum Aspect Ratio
6032	Hybrid Resistor Maximum Aspect Ratio
6033	Hybrid Resistor Trim to Conductor Clearance
6034	Hybrid Resistor Default Direction
6035	Hybrid Resistor Required Direction
6036	Hybrid Resistor Required Layer
6037	Hybrid Resistor Ink Deviation (Length)
6038	Hybrid Resistor Ink Deviation (Percent of Deviation)

#### Electrical and LEP Manufacturing Attribute List

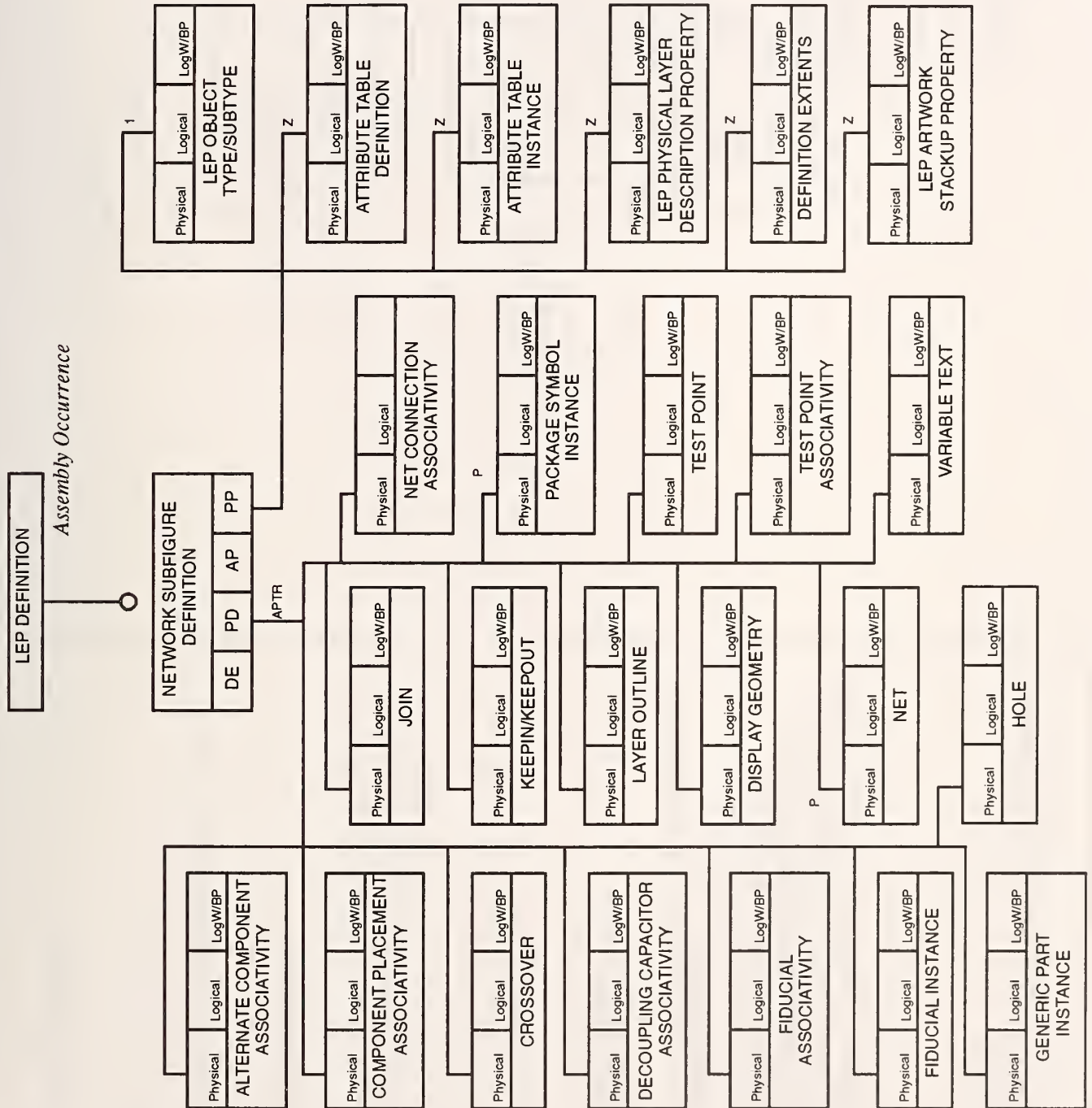
20	Electrostatic Discharge Rating
22	LEP Design Thickness

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



5.3.2.28 LEP Fixed Component Placement Property

Description:

The Fixed Component Placement Property object maps directly to the IGES LEP Fixed Component Placement Property (Type 406 Form 5xxx). Please refer to the IGES specification for additional information.

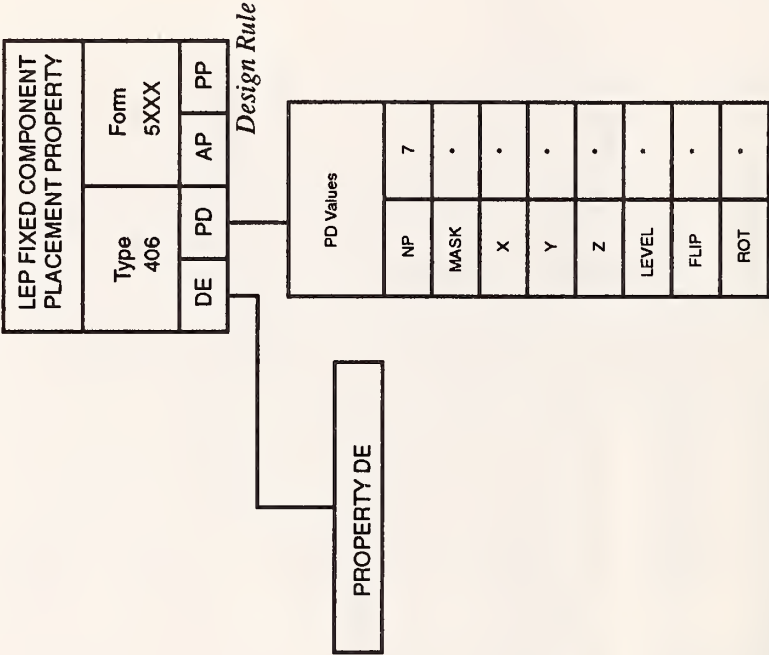
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.2.29 LEP Instance

#### Description:

The LEP Instance object is an instantiation of a LEP Definition.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Network Subfigure Instance object, must specify (*otype*=Layered\_Electrical\_Product, *stype*=\*).
5. The following Attribute Table objects can be referenced from the LEP Instance:

#### Electrical Attribute List

6024 Generic Design Rule

#### Electrical & LEP Manufacturing Attribute List

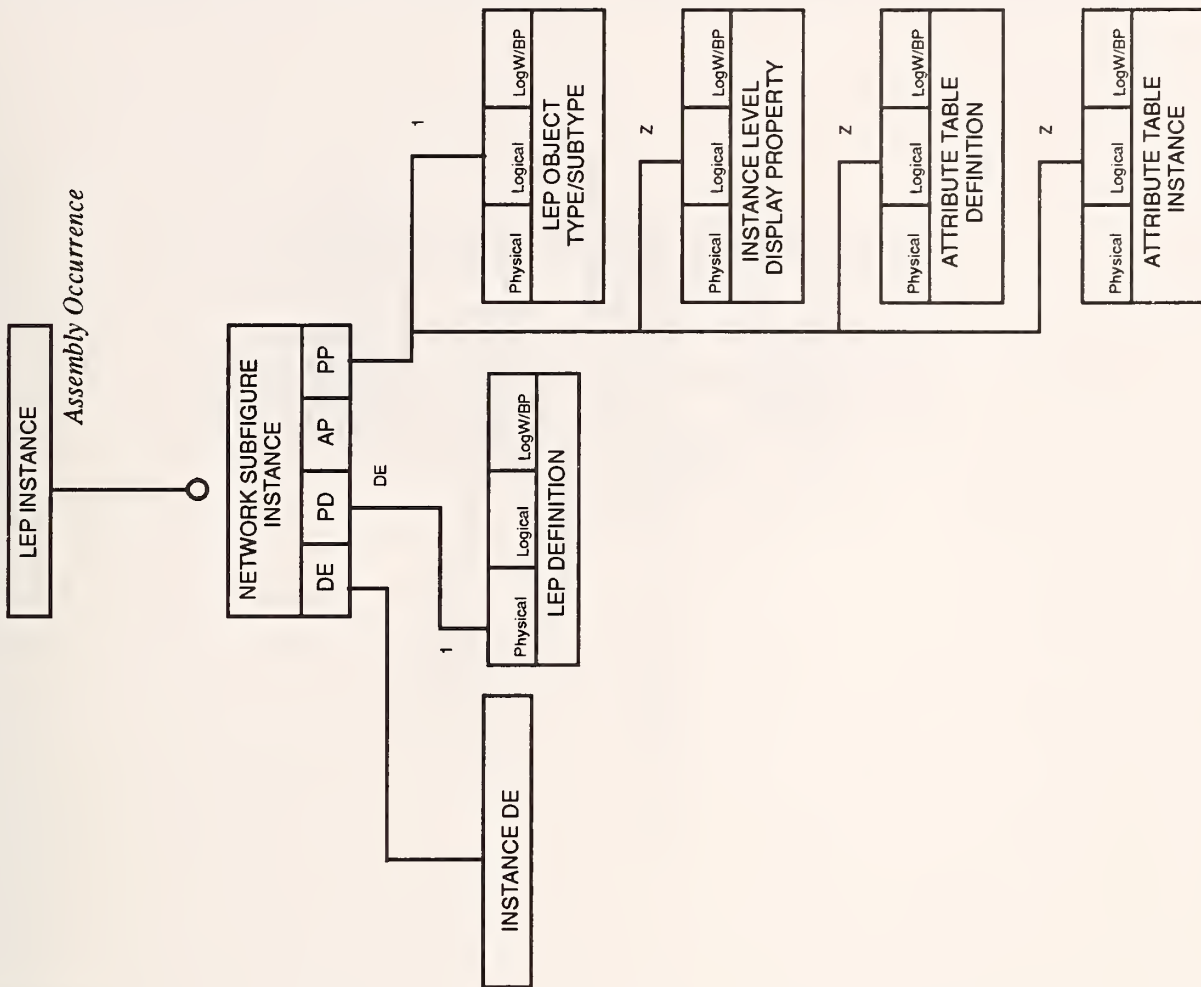
- 1 Component Physical Orientation
- 3 Component Physical Thickness
- 20 Electrostatic Discharge Rating
- 22 LEP Design Thickness

#### Translation Usage Notes:

**General:**

**Output:**

**Input:**



### 5.3.2.30 LEP Object Type/Sub-Type

#### Description:

The Object Type/Sub-Type Property object maps directly to the IGES LEP Object Type/Sub-Type Property (Type 406 Form 5xxx). Please refer to the IGES specification for additional information.

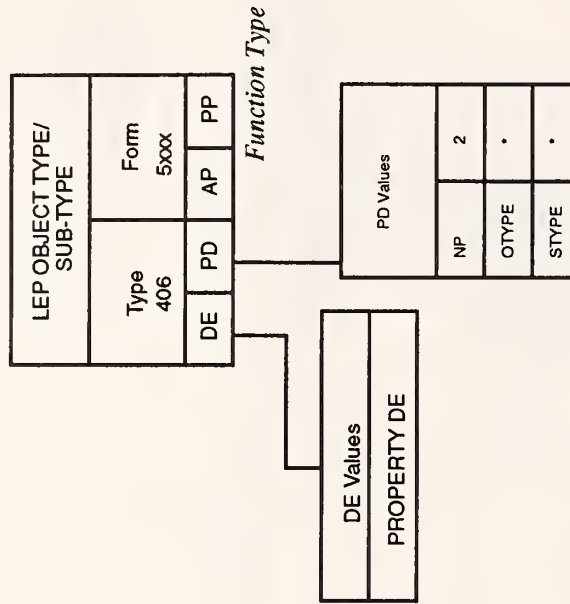
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



5.3.2.31 LEP Physical Layer Description

Description:

The LEP Physical Layer Description object maps directly to the IGES LEP Physical Layer Description Property (Type 406 Form 5xxx). Please refer to the IGES specification for additional information.

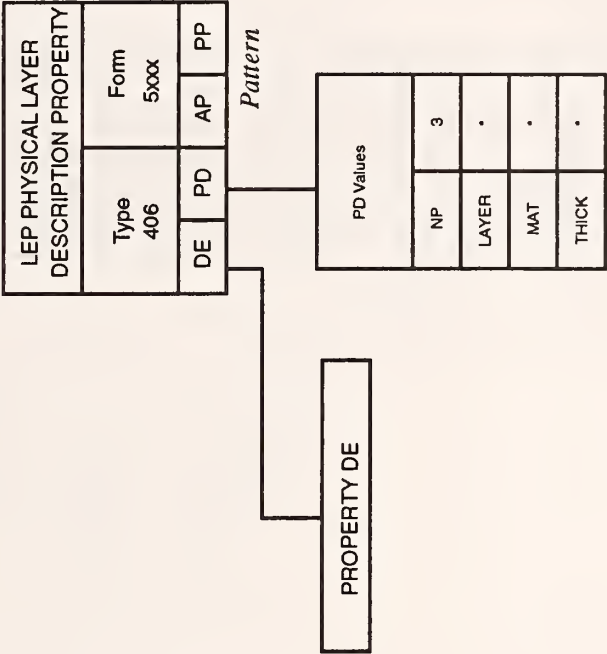
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.2.32 LEP Substrate Hole Property

#### Description:

The LEP Substrate Hole Property object maps directly to the IGES LEP Substrate Hole Property (Type 406 Form 26). Please refer to the IGES specification for additional information.

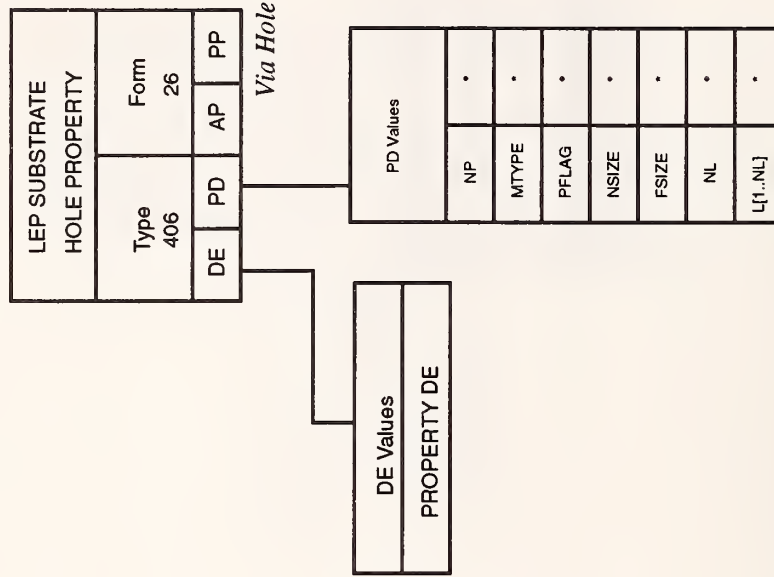
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



5.3.2.33 Level to LEP Map

Description:

The Level To LEP Layer Map object maps directly to the IGES Level To LEP Layer Map Property (Type 406 Form 24). Please refer to the IGES specification for additional information.

Requirements/Restrictions:

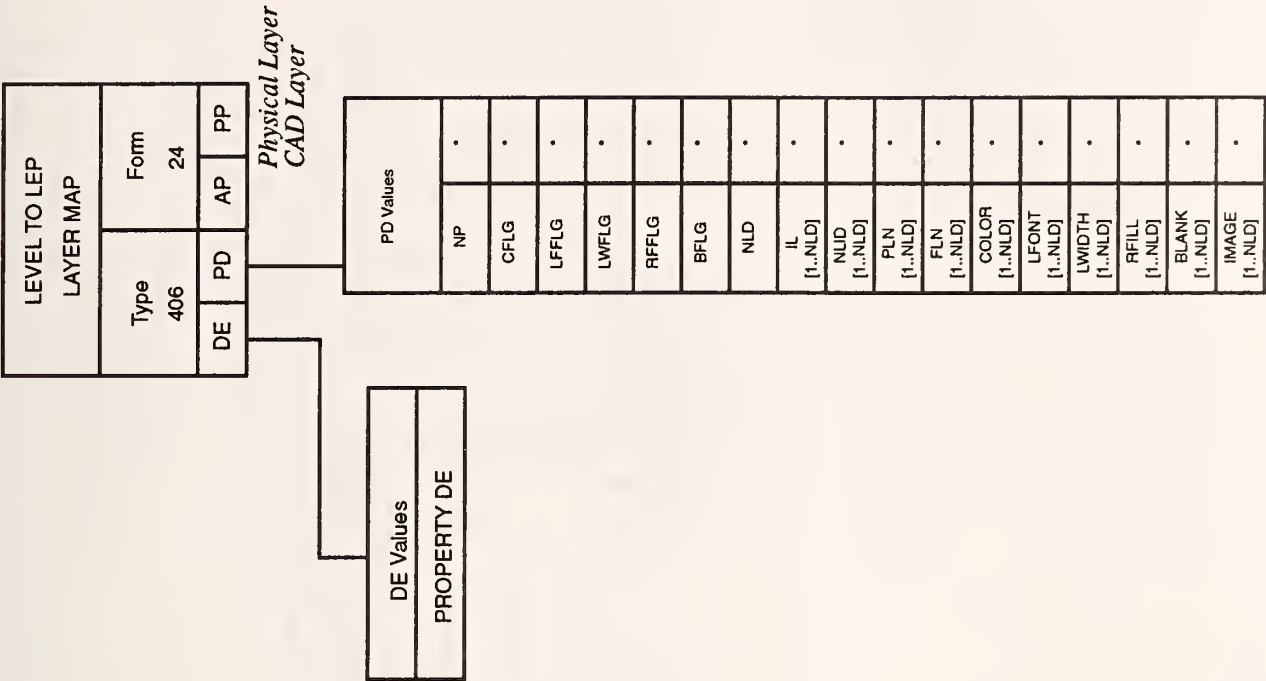
- 4. The Level To LEP Layer Map is always independent (DE Attribute Subordination equals 0) within the IGES file, thus it pertains to all other entities in the file.

Translation Usage Notes:

General:

Output:

Input:



### 5.3.2.34 Machined Hole

**Description:**

The LEP Machined Hole object specifies the location and characteristics of a hole in the LEP that requires some type of machining process to be created (i.e., drilling, milling, etc.).

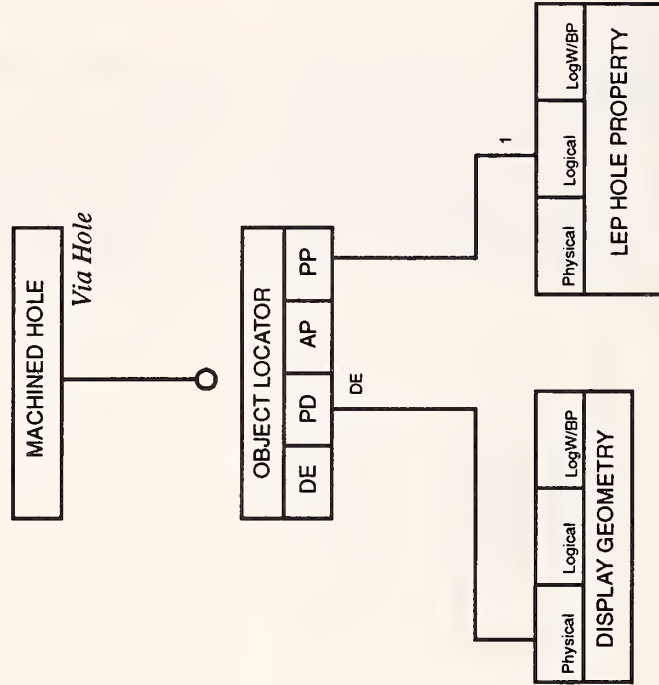
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



# 5.3.2.35 Machined Hole Figure Associativity

## Description:

The Machined Hole Figure Associativity object associates a Machined Hole with it's corresponding Machined Hole Figure.

## Requirements/Restrictions:

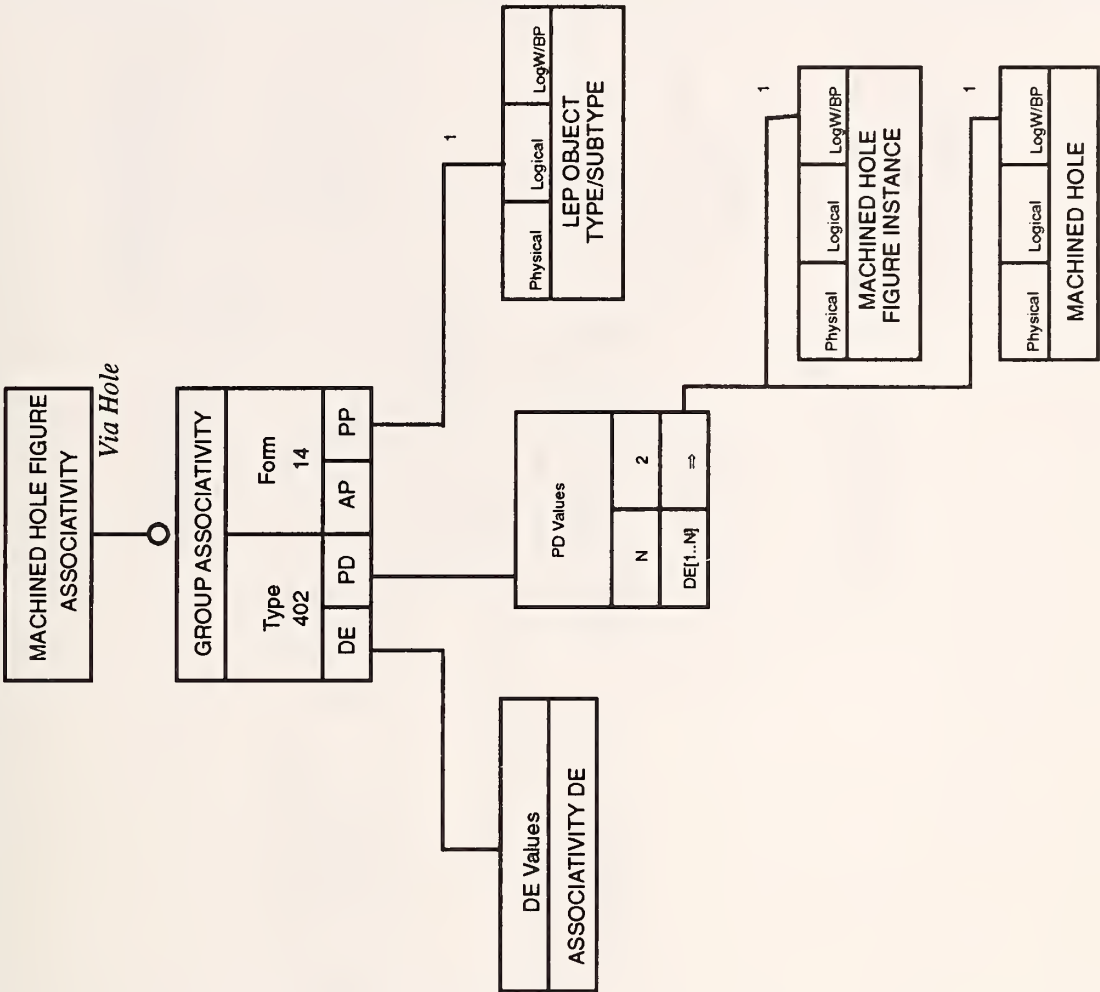
- 4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*otype*=Machined\_Hole\_Figure\_Associativity, *stype*=\*).
- 5. The first object referenced from the Group Associativity must be the Machined Hole Figure Instance, followed by the Machined Hole.
- 6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

## Translation Usage Notes:

### General:

### Output:

### Input:



### 5.3.2.36 Machined Hole Figure Definition

**Description:**

The Machined Hole Figure Definition object is a Subfigure Definition, which contains the display geometry objects that define a machine hole figure. A machine hole figure is a symbol which is used to help visually recognize where certain machined holes are located.

**Requirements/Restrictions:**

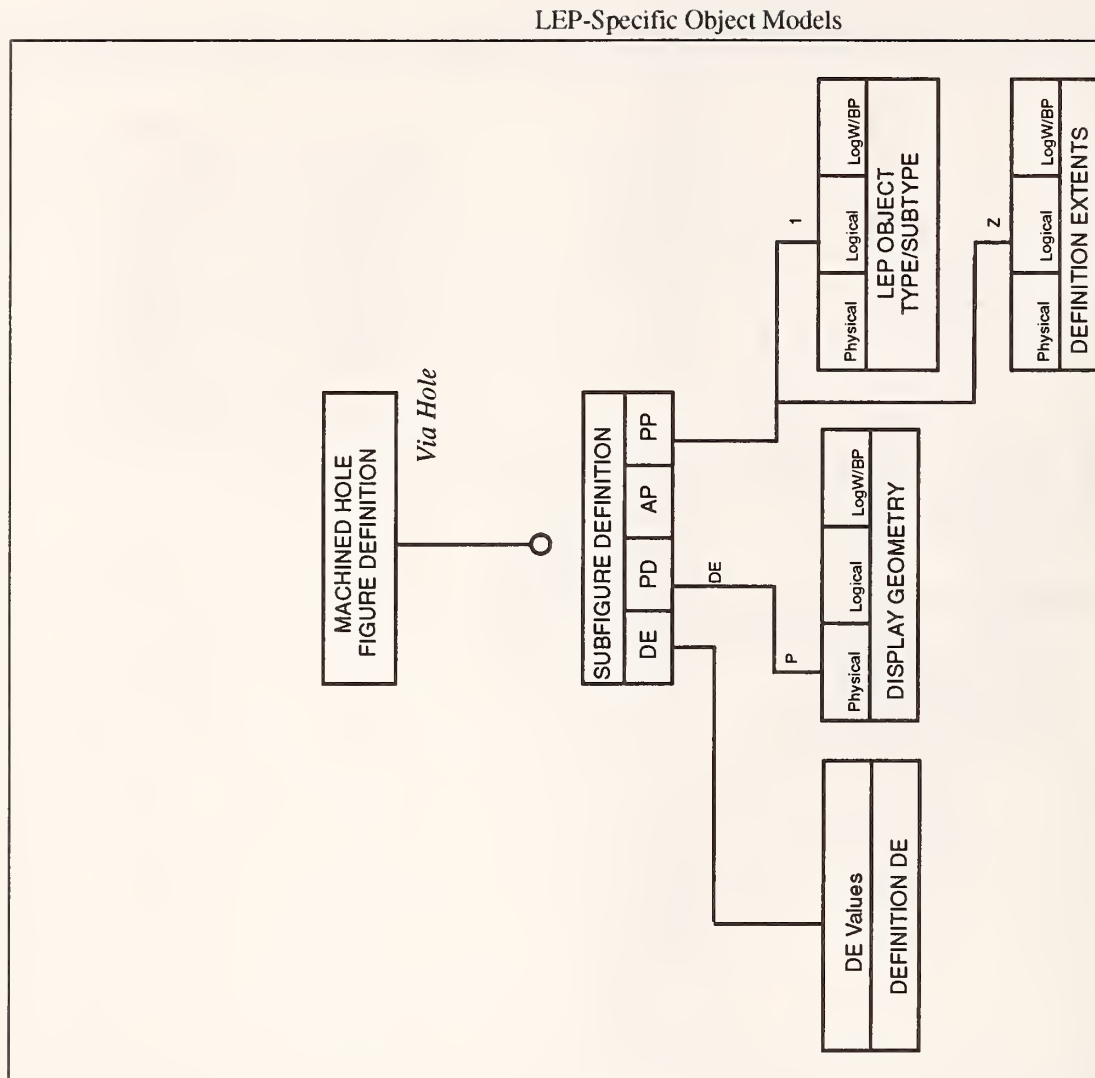
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype*=Machined\_Hole\_Figure, *stype*=\*).
5. The NAME field in the Subfigure Definition must be unique (for all Machined Hole Figure Definitions) within the scope of the IGES File.

### Translation Usage Notes:

### General:

**Output:**

**Input:**



### 5.3.2.37 Machined Hole Figure Instance

#### Description:

The Machined Hole Figure Instance object is an instantiation of a Machined Hole Figure Definition.

#### Requirements/Restrictions:

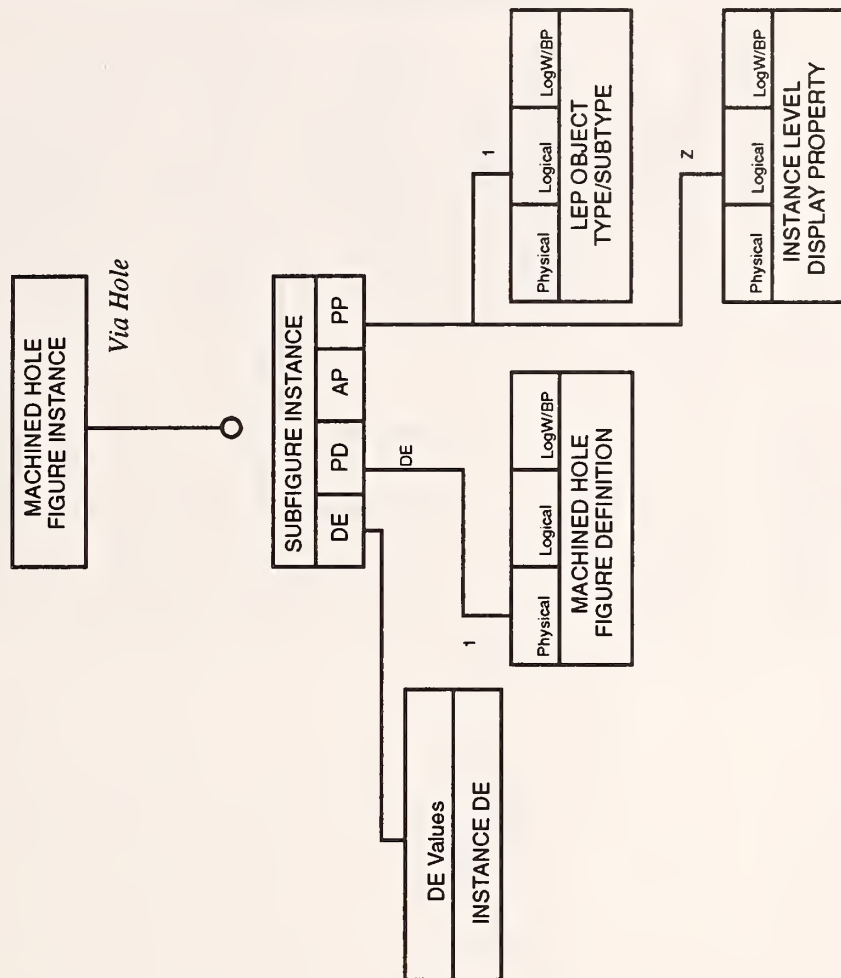
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (*otype*=Machined\_Hole\_Figure, *stype*=\*).
5. The Machined Hole Figure Instance can be implemented using either a Subfigure Instance or a Modified Subfigure Instance.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



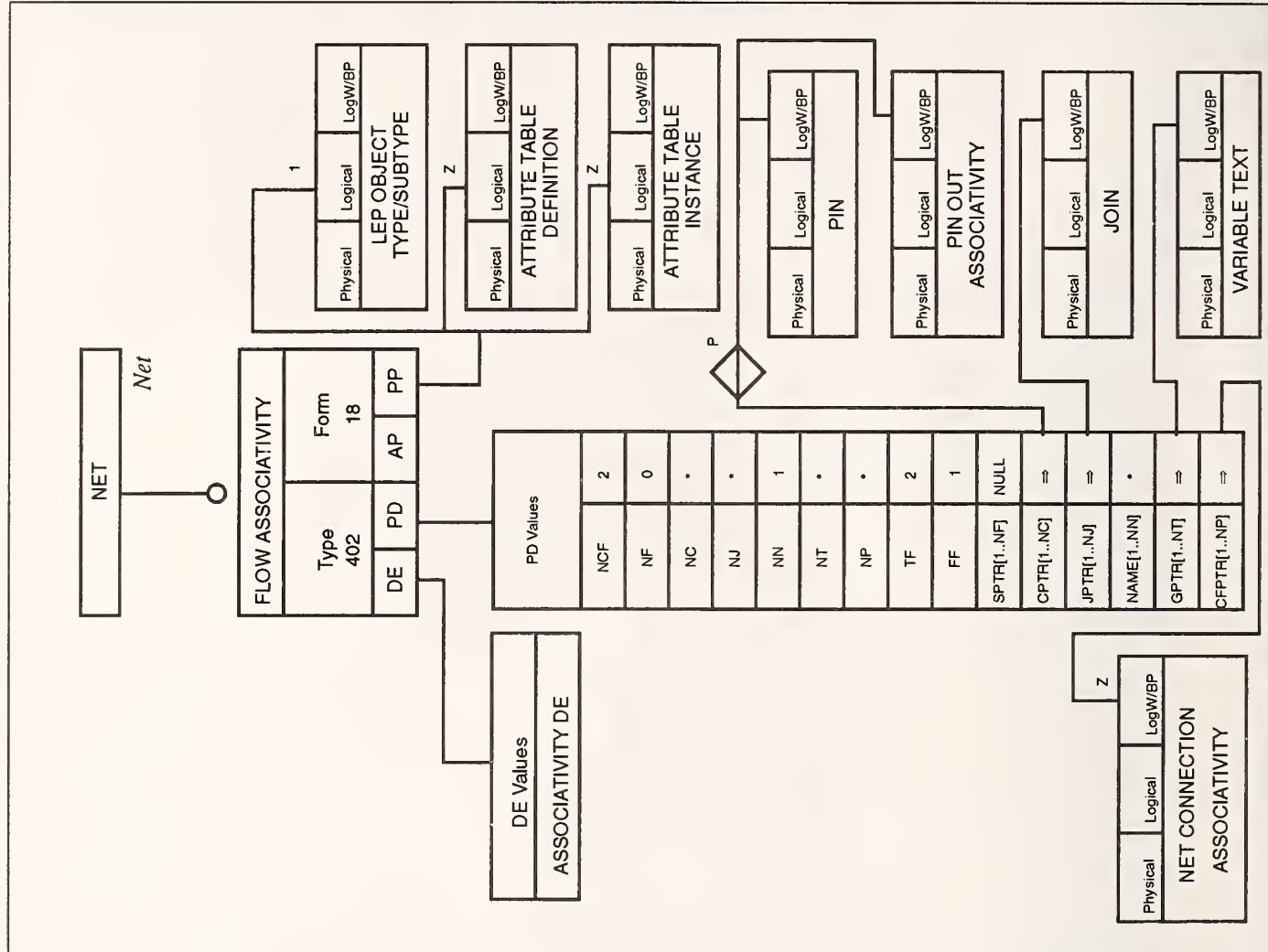
### 5.3.2.38 Net

#### Description:

The Net object associates all of the electrically common pins and physical join geometry (i.e., conductive filled areas, conductive paths and vias). The Net is intended to represent the LEP design net. If you are concerned with the substrate net you must analyze the structure of the Joins to determine which Pins are electrically connected at the substrate level (i.e., not through the use of Jumper Wires).

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Network Flow Associativity object, must specify (*otype*=Net, *stype*=\*).
5. The NAME field in the Network Flow Associativity must be unique (For all Nets) within the scope of the LEP Definition.
6. Pins can be referenced by either a Pin object or a Pin Out Associativity object.
7. All objects that are subordinate to the Network Flow Associativity (with the exception of Pins and Pin Out Associativities), are physically dependent on the same parent as the Network Flow Associativity.
8. There must be 2 or more Pin or Pin Out Associativity objects subordinate to the Net.
9. If the LEP is not routed or only partially routed the Net Connection Associativity does not need to be



used. However, if the LEP is completely routed (all Net Pins are physically connected), then the Net Connection Associativity is required.

10. The following Attribute Table objects can be referenced from the Net:

**Electrical Attribute List**

6017	Net Length Rule
6018	ECL Net Length Rule
6019	Net Order Rule
6020	Net Priority
6021	Net Source Pin Rule
6022	Net Restrictions Rule
6023	Net Terminating Resistor Rule
6024	Generic Design Rule

85 **Translation Usage Notes:**

**General:**

The Variable Text object is used to specify the net name or identification.

**Output:**

**Input:**

### 5.3.2.39 Net Connection Associativity

#### Description:

The Net Connection Associativity object defines the order of the joins within a Net. By analyzing the Net Connection Associativity, you can determine the exact physical path that electricity will move on a pin by pin and join by join basis.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Net Connection Associativity object, must specify (*otype*=Net\_Connection\_Associativity, *stype*=\*).

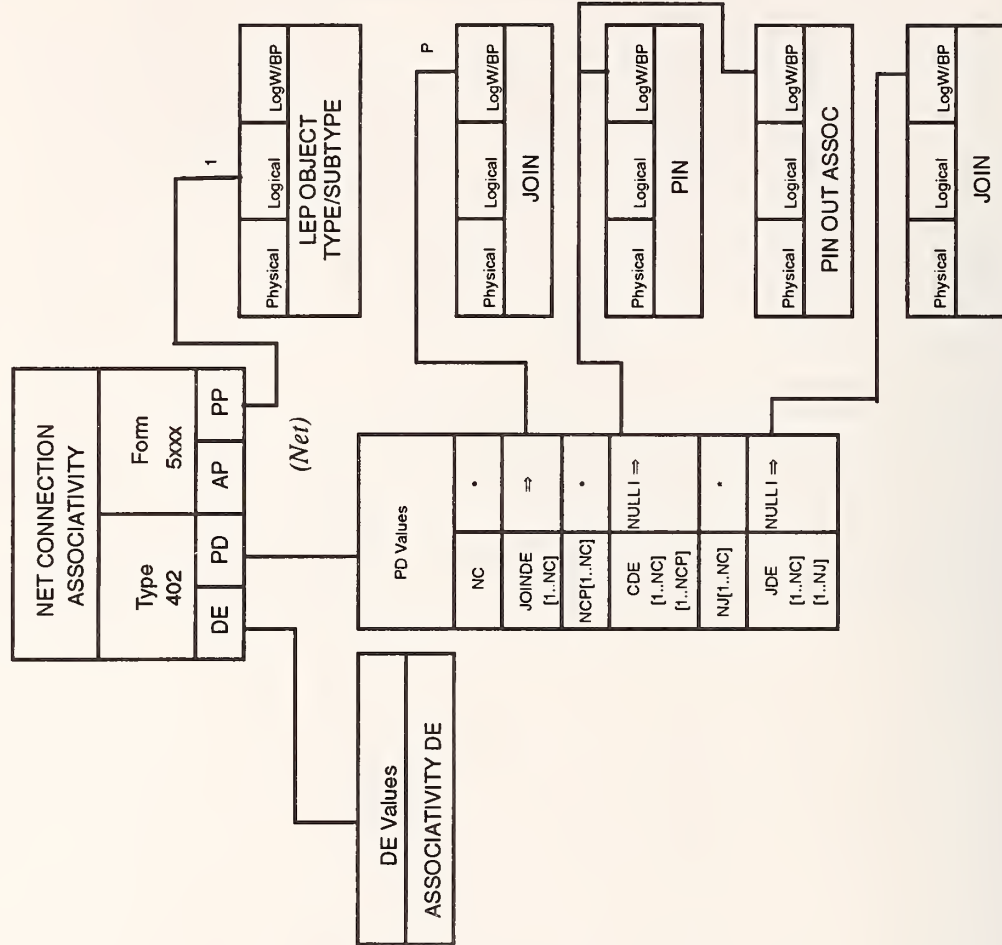
8

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.2.40 Package Symbol Definition

#### Description:

The Package Symbol Definition object is a Network Subfigure Definition, which specifies all of the constituent objects, that are required to define a footprint in the LEP, which can support the attachment of a physical component.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Network Subfigure Definition object, must specify (*otype*=Package\_Symbol, *stype*=\*).
5. A Routing Keepin or Placement Keepin cannot be subordinate to a Package Symbol Definition.
6. The NAME field in the Network Subfigure Definition must be unique (for all Package Symbol Definitions) within the scope of the IGES File.
7. The following Attribute Table objects can be referenced from the Package Symbol Definition:

#### Electrical Attribute List

5001	Hybrid Resistor Laser Trim Value
5002	Hybrid Resistor Laser Trim Process
5003	Hybrid Resistor Ink ID
5004	Hybrid Resistor Shape
5005	Hybrid Resistor Length
5006	Hybrid Resistor Width
5007	Hybrid Resistor Hat Length

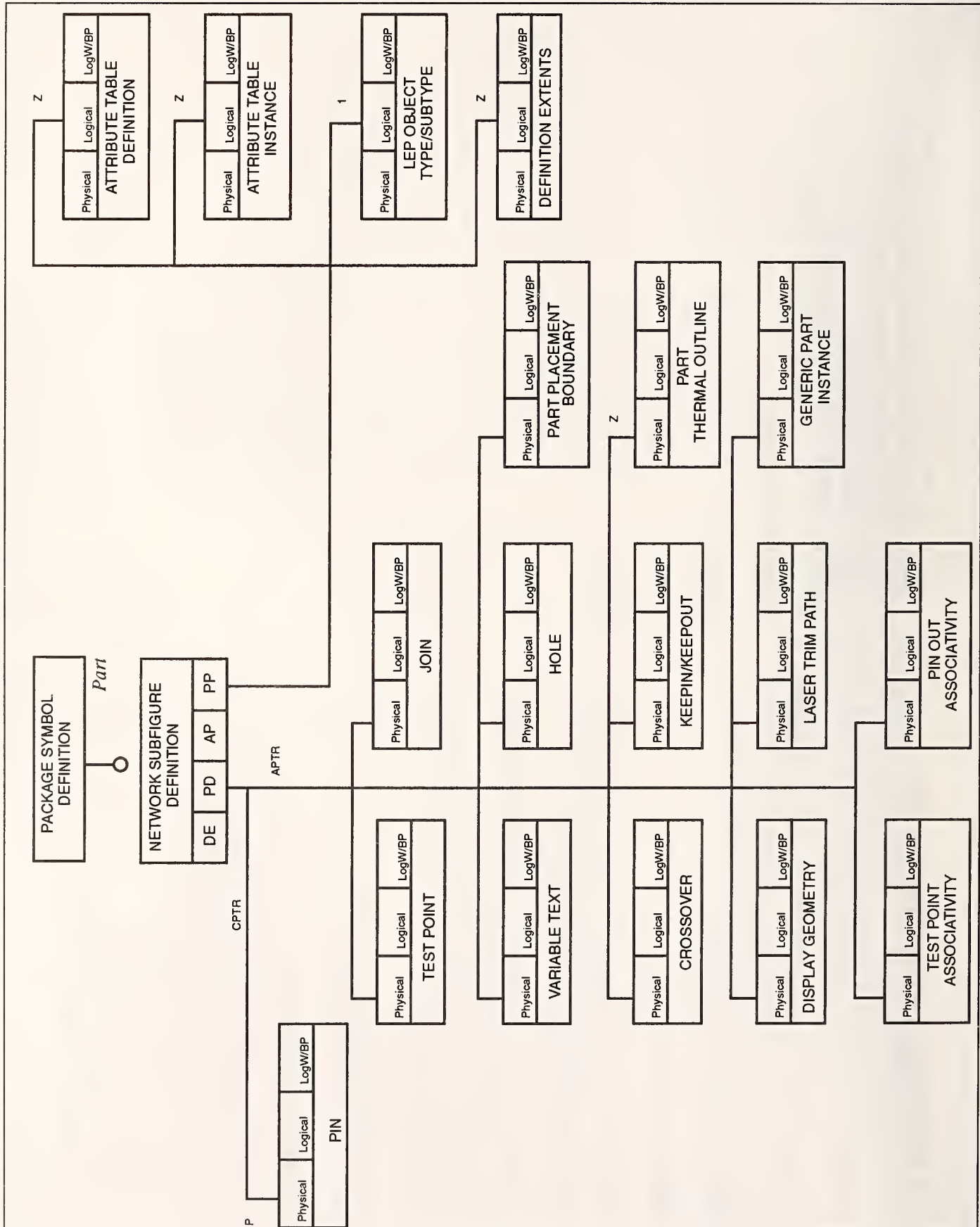
5008	Hybrid Resistor Hat Width
5009	Hybrid Resistor Terminal Length Extension
5010	Hybrid Resistor Terminal Width Extension
5011	Hybrid Resistor Terminal Overlap
6024	Generic Design Rule
6025	Component Pins Modified Rule

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.2.41 Package Symbol Instance

#### Description:

The Package Symbol Instance object is an instantiation of a Package Symbol Definition.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Modified Network Subfigure Instance object, must specify (*otype*=Package\_Symbol, *stype*=\*).
5. The PRD field in the Modified Network Subfigure Instance must be unique within the scope of the LEP Definition.
6. If the Package Symbol Instance has not been modified, the MDE pointer should be 0 or null.
7. The following Attribute Table objects can be referenced from the Package Symbol Instance:

#### Electrical Attribute List

23	Capacitance
43	Conductance
130	Impedance
132	Inductance
239	Power
240	Power Dissipation
281	Resistance
285	Resistivity
355	Temperature
396	Voltage

5001	Hybrid Resistor Laser Trim Value
5002	Hybrid Resistor Laser Trim Process
5003	Hybrid Resistor Ink ID
5004	Hybrid Resistor Shape
5005	Hybrid Resistor Length
5006	Hybrid Resistor Width
5007	Hybrid Resistor Hat Length
5008	Hybrid Resistor Hat Width
5009	Hybrid Resistor Terminal Length Extension
5010	Hybrid Resistor Terminal Width Extension
5011	Hybrid Resistor Terminal Overlap
6024	Generic Design Rule

#### Electrical and LEP Manufacturing Attribute List

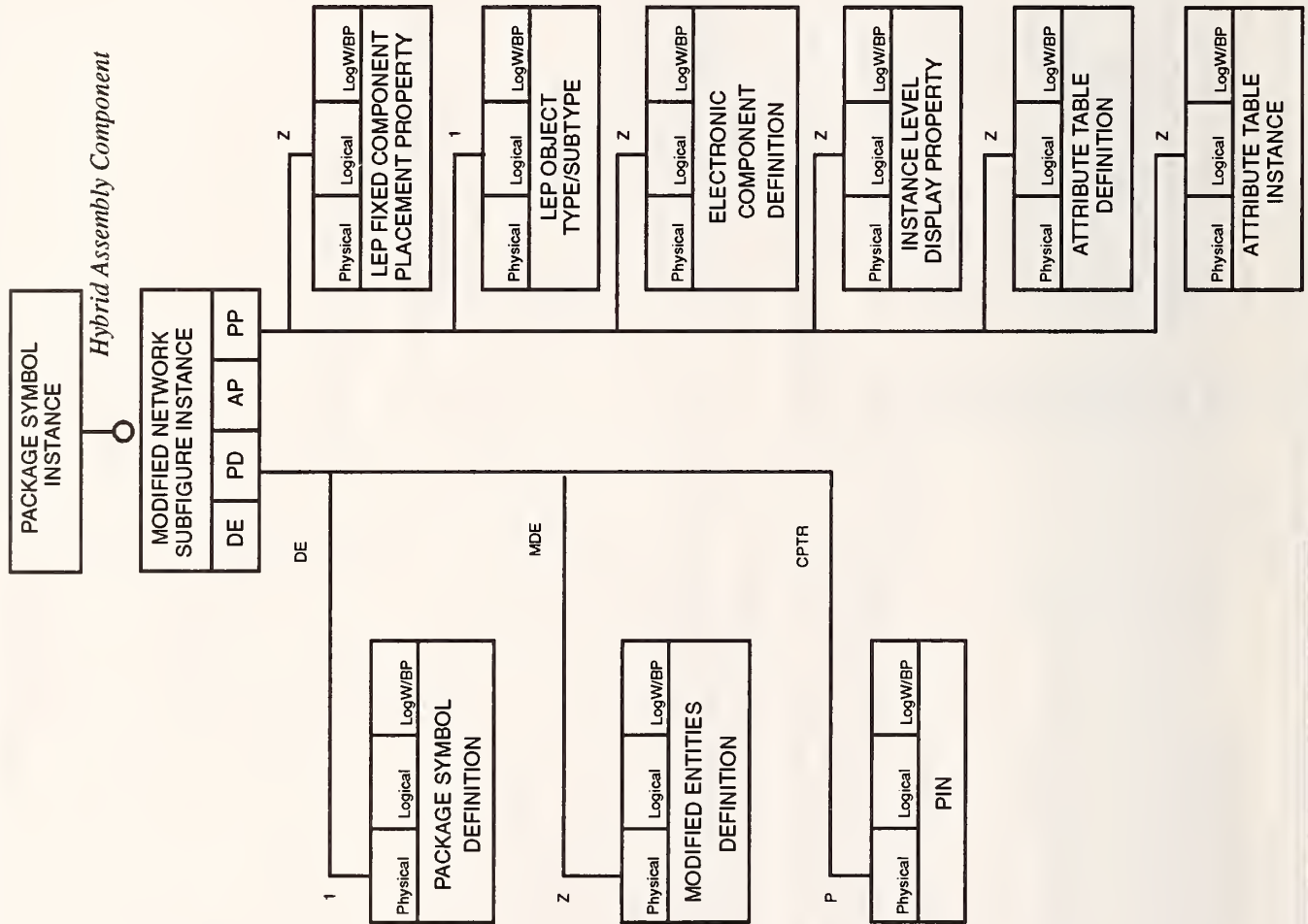
1	Component Physical Orientation
3	Component Physical Thickness
4	Component Placement Lead Forming
5	Component Placement Depth Stop
6	Component Placement Force
7	Component Placement Machine
8	Component Placement Tool
9	Component Placement Feeder Machine
10	Component Placement Feeder Location
20	Electrostatic Discharge Rating

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



## 5.3.2.42 Padstack Definition

### Description:

The Padstack Definition object is a Subfigure Definition, which specifies all of the constituent objects, that are required to define the characteristics of the area in which a package symbol is electrically connected to the LEP.

The characteristics of each layer that is associated with the padstack must be defined within the Padstack Definition.

### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype*=Padstack, *stype*=\*).
5. The NAME field in the Subfigure Definition must be unique (for all Padstack Definitions) within the scope of the IGES File.

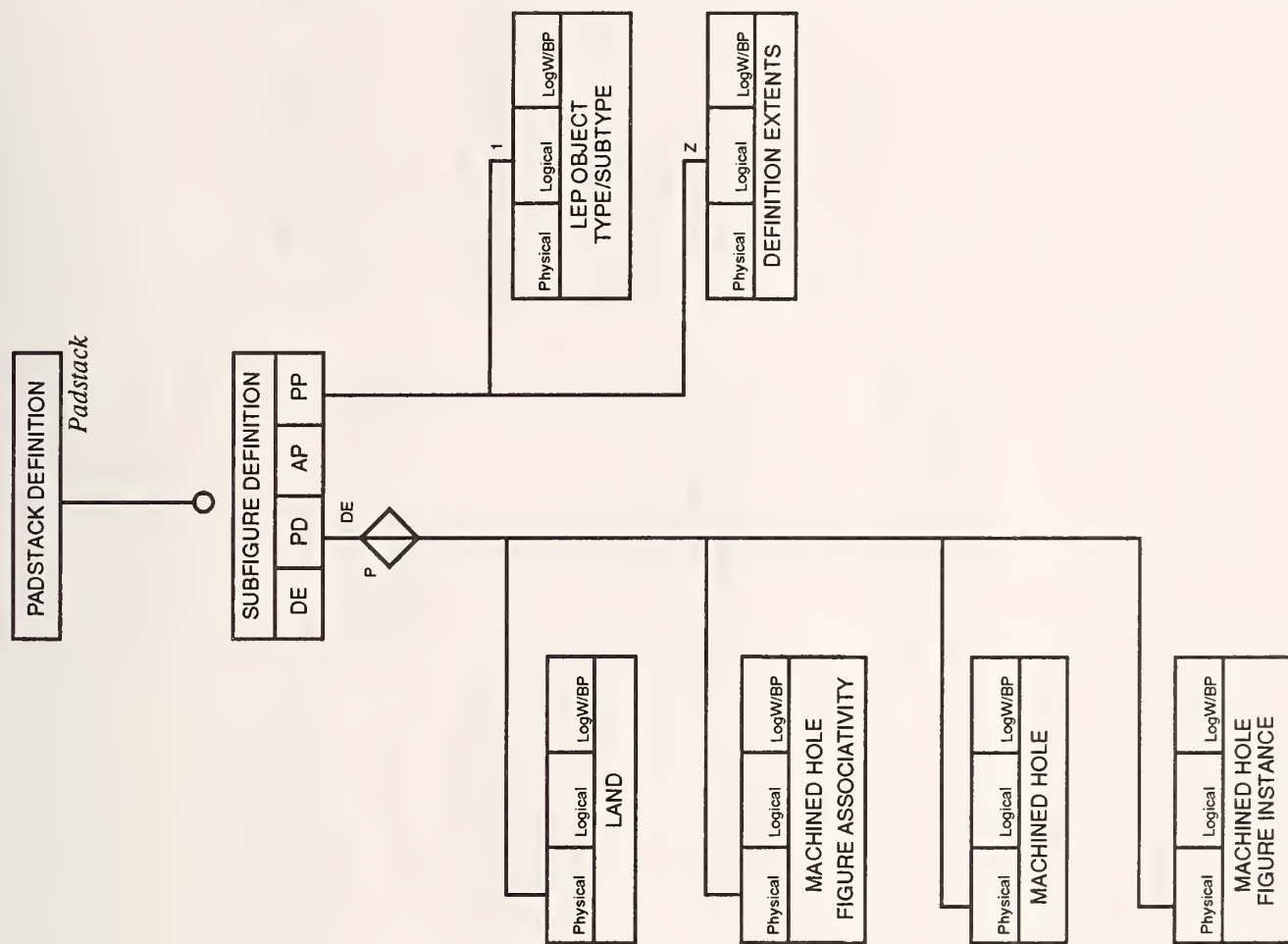
### Translation Usage Notes:

#### General:

The DE Level attribute is used to specify which levels (physical layers) the padstack encompasses. In order to specify more than one level, a Level Definition object should be used.

#### Output:

#### Input:



### 5.3.2.43 Padstack Instance

#### Description:

The Padstack Instance object is an instantiation of a Padstack Definition.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Modified Subfigure Instance object, must specify (*otype*=Padstack, *stype*=\*).
5. If the Padstack Instance has not been modified, the MDE pointer should be 0 or null.

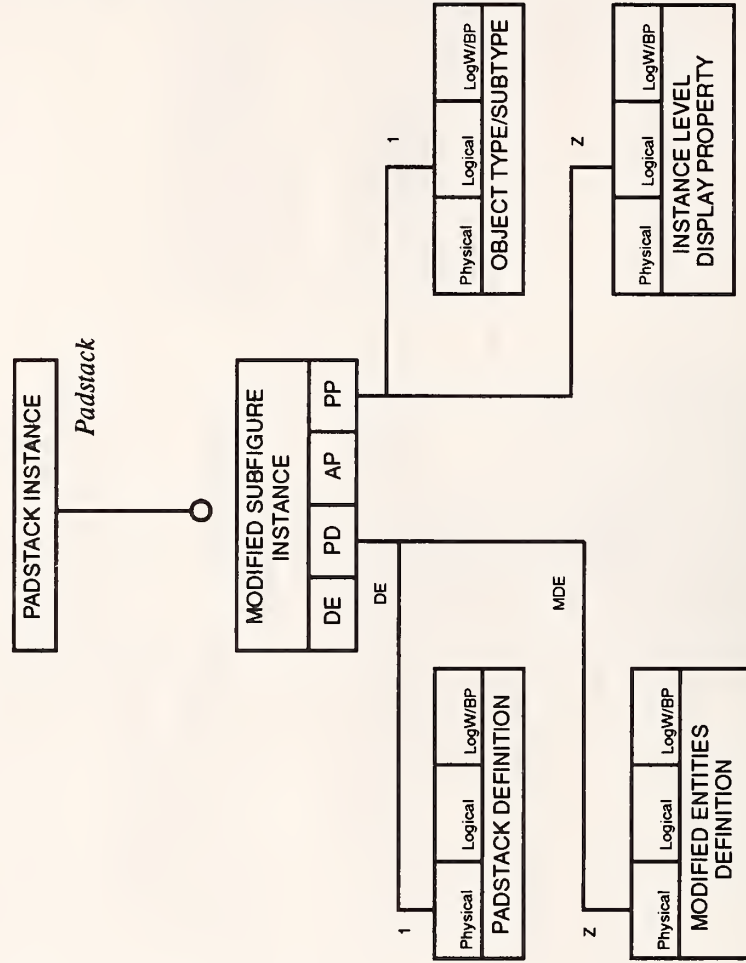
#### Translation Usage Notes:

##### General:

The DE Level attribute is used to specify which levels (physical layers) the padstack encompasses. In order to specify more than one level, a Level Definition object should be used.

##### Output:

##### Input:



# 5.3.2.44 Panel Definition

## Description:

The Panel Definition object is a Subfigure Definition, which specifies all of the constituent objects that are required to define a manufacturing panel.

## Requirements/Restrictions:

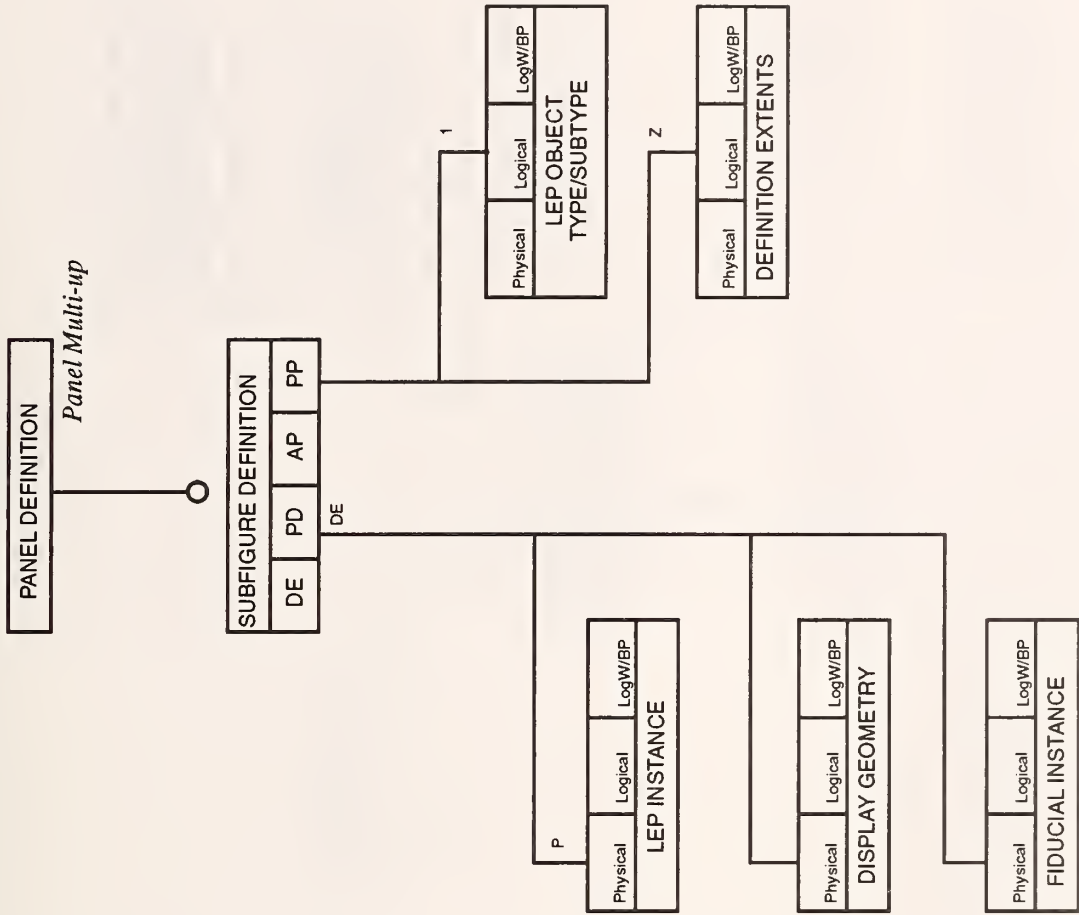
- 4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype*=Panel, *stype*=\*).
- 5. The NAME field in the Subfigure Definition must be unique (for all Panel Definitions) within the scope of the IGES File.

## Translation Usage Notes:

### General:

### Output:

### Input:



### 5.3.2.45 Panel Instance

#### Description:

The Panel Instance object is an instantiation of a Panel Definition.

#### Requirements/Restrictions:

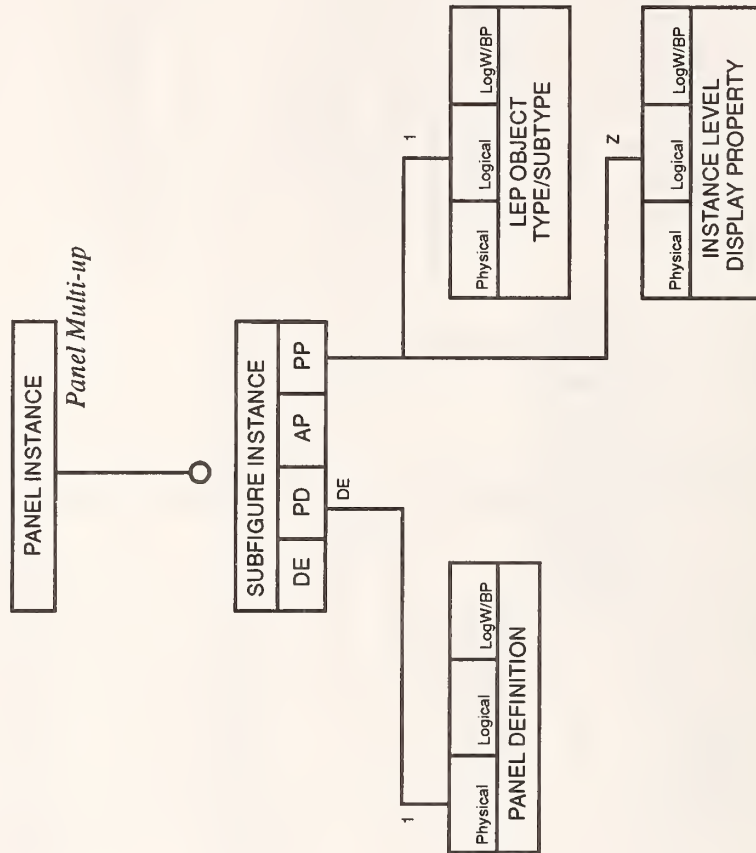
4. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (*otype=Panel, stype=\**).
5. The Panel Instance can be implemented using either a Subfigure Instance or a Modified Subfigure Instance.

#### 24 Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.2.46 Pin

**Description:**

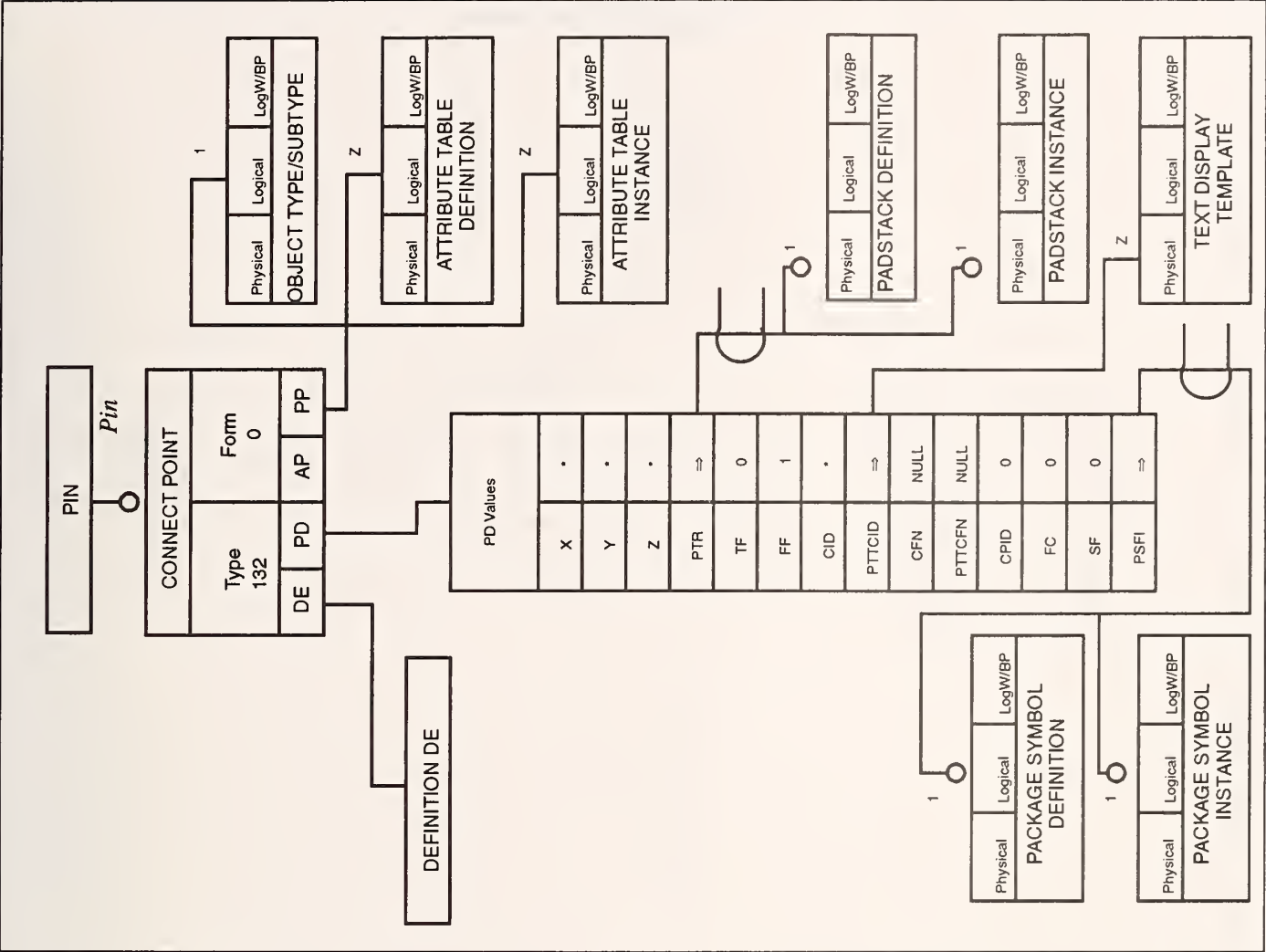
The Pin object specifies the location, and functional characteristics of where a package symbol is electrically connected to the LEP.

**Requirements/Restrictions:**

- 4. The LEP Object Type/Sub-Type property, which is referenced from the Connect Point object, must specify (*otype*=Pin, *stype*=\*).
- 5. The LEP Object Type/Sub-Type property, which is referenced from the Connect Point object, must specify (*otype*=Pin, *stype*=\*).
- 6. There is no subordination associated with the PSFI pointer. It is an informational reference only.
- 7. The CID field in the Connect Point must be unique within the scope of the Package Symbol Definition or Package Symbol Instance.
- 8. The following Attribute Table objects can be referenced from the Pin:

**Electrical Attribute List**

- 234 Pin Size
- 6024 Generic Design Rule



**Electrical and LEP Manufacturing Attribute List**

4      Component Placement Lead Forming

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**

### 5.3.2.47 Pin Out Associativity

**Description:**

The Pin Out Associativity object associates a Pin and a set of one or more Joins. It is used to specify a certain “fan-out” pattern for a Package Symbol Definition that has a very small pitch between it's pins.

**Requirements/Restrictions:**

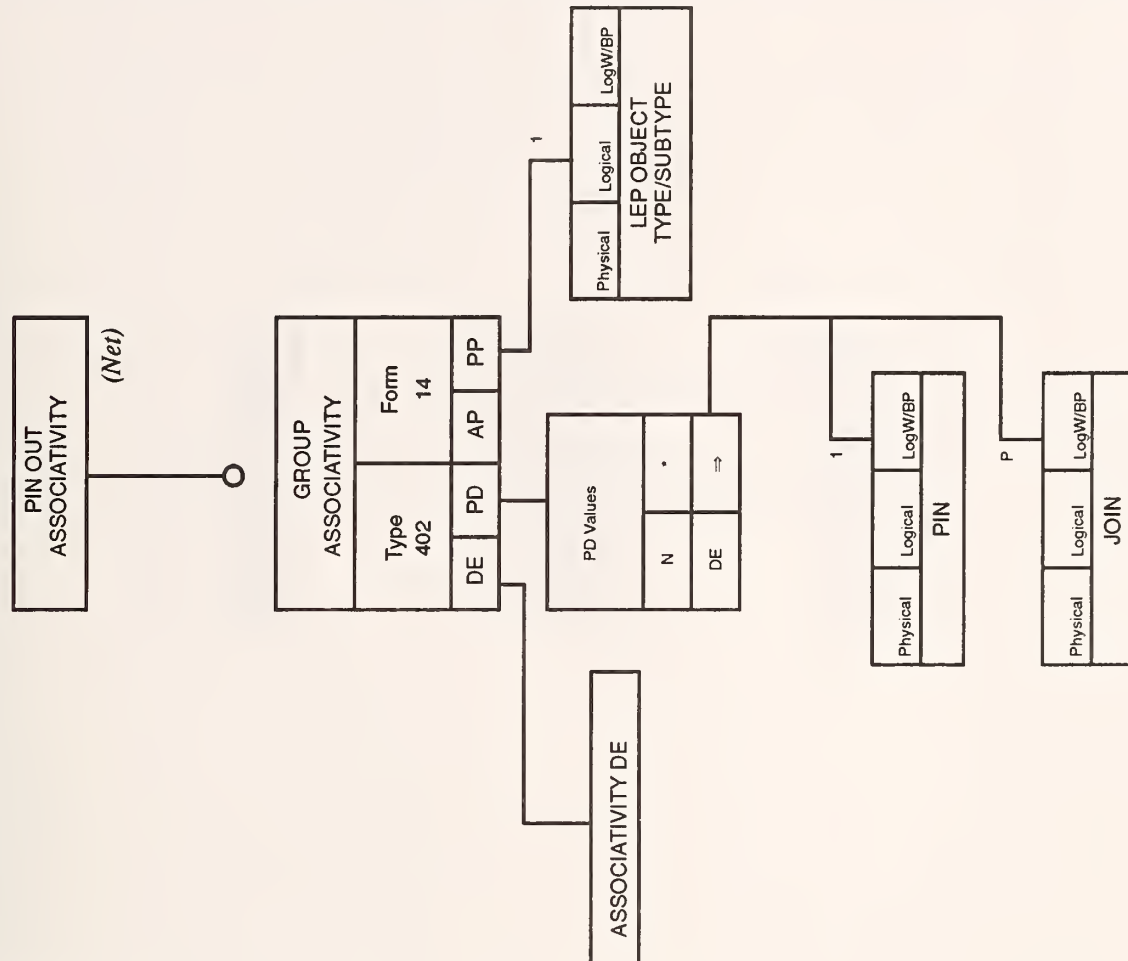
4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*type*=Pin\_Out\_Associativity, *type*=\*).
5. The first object referenced from the Group Associativity must be the Pin, followed by one or more Joins.
6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

### Translation Usage Notes:

## General:

**Output:**

## Input:



### 5.3.2.48 Routing Keepin

**Description:**

The Routing Keepin object is a closed curve, which represents an outline in which all routing (i.e., conductive filled areas, conductive paths, and vias) must be within.

**Requirements/Restrictions:**

**Translation Usage Notes:**

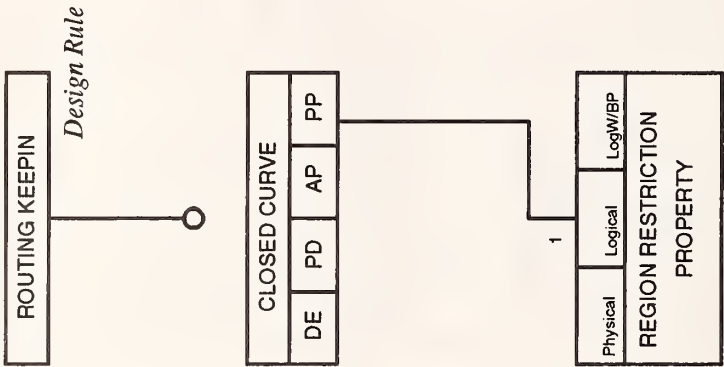
**General:**

The values for the Region Restriction Property should be as follows;

- VR=0
- CR=0
- TR=0
- RR=1

**Output:**

**Input:**



### 5.3.2.49 Routing Keepout

**Description:**

The Routing Keepout object is a closed curve, which represents an outline in no routing (i.e., conductive filled areas, conductive paths, and vias) is allowed.

**Requirements/Restrictions:**

**Translation Usage Notes:**

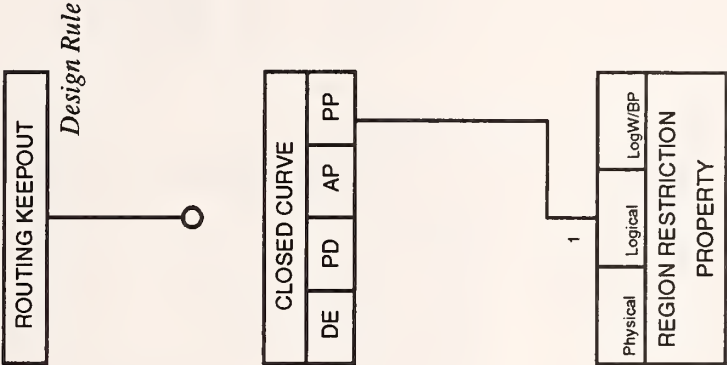
**General:**

The values for the Region Restriction Property should be as follows;

- VR=0
- CR=0
- TR=0
- RR=2

**Output:**

**Input:**



### 5.3.2.50 Test Point

#### Description:

The Test Point object represents a location which is designated for probing during a specific electrical test procedure (i.e., in-circuit, bare board, functional, etc.).

#### Requirements/Restrictions:

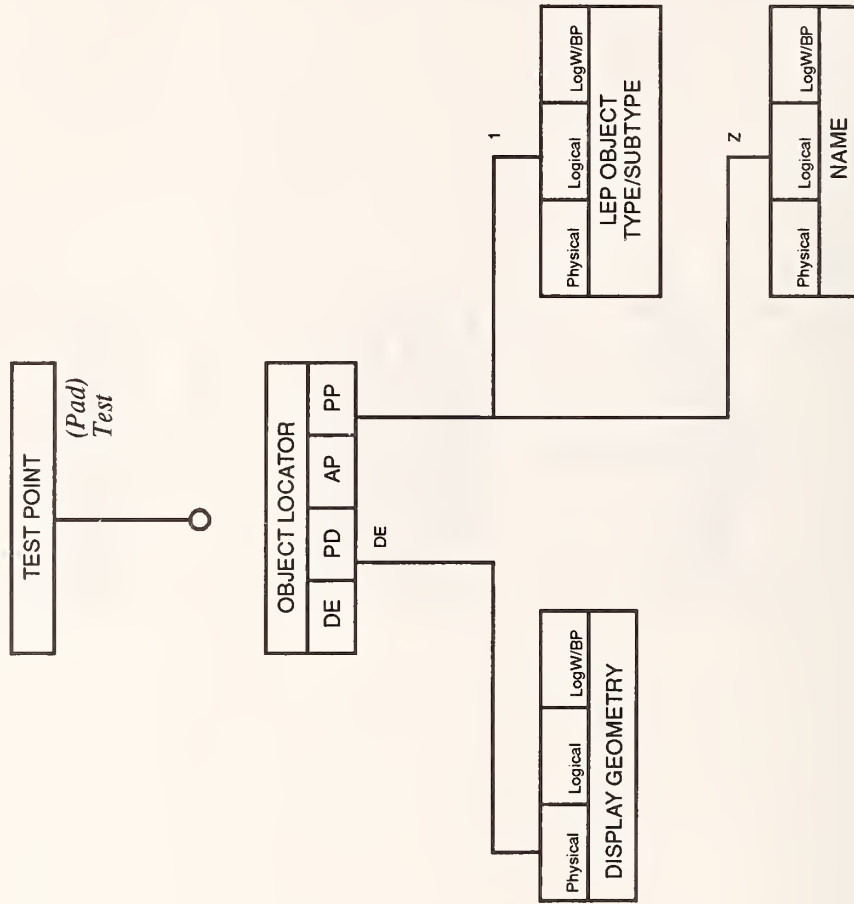
4. The LEP Object Type/Sub-Type property, which is referenced from the Object Locator object, must specify (*otype=Test\_Point, subtype=\**).

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.2.51 Test Point Associativity

#### Description:

The Test Point Associativity object associates a Test Point and a corresponding Pin, Net or Join.

#### Requirements/Restrictions:

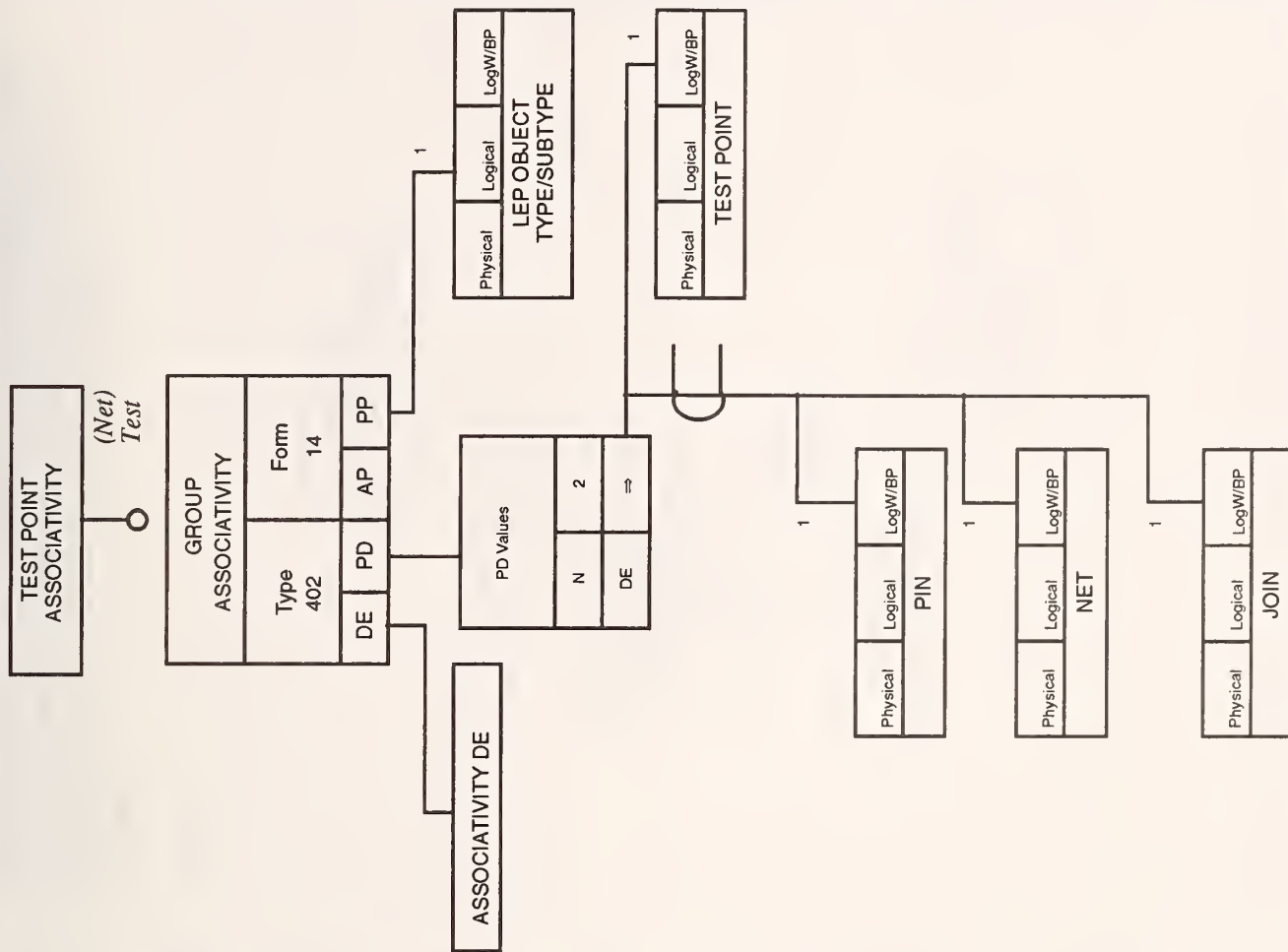
4. The LEP Object Type/Sub-Type property, which is referenced from the Group Associativity object, must specify (*otype*=Test\_Point\_Associativity, *stype*=\*).
5. The first object referenced from the Group Associativity must be the Test Point, followed by either a Pin, Net or Join.
6. All objects that are subordinate to the Group Associativity, are physically dependent on the same parent as the Group Associativity.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.2.52 Trace Keepout

#### Description:

The Trace Keepout object is a closed curve, which represents an outline in which no traces (i.e., conductive areas or conductive paths) are allowed.

#### Requirements/Restrictions:

#### Translation Usage Notes:

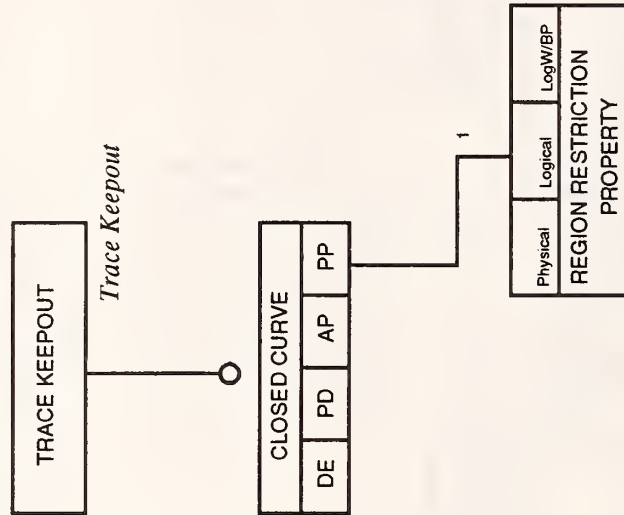
#### General:

The values for the Region Restriction Property should be as follows;

VR=0  
CR=0  
TR=2  
RR=0

#### Output:

#### Input:



### 5.3.2.53 Variable Text

#### Description:

The Variable Text object represents a unique Text String, which is associated to some functional value for the parent object (i.e., part number, component type, component value, etc.). The Variable Text is used as a template in a definition object. Upon instantiation of the definition, the actual value gets plugged into the template. In many cases the location of the Text String is modified upon instantiation.

#### Requirements/Restrictions:

4. The LEP Object Type/Sub-Type property, which is referenced from the Text String object, must specify (*otype*=Variable\_Text, *stype*=\*).

#### Translation Usage Notes:

#### General:

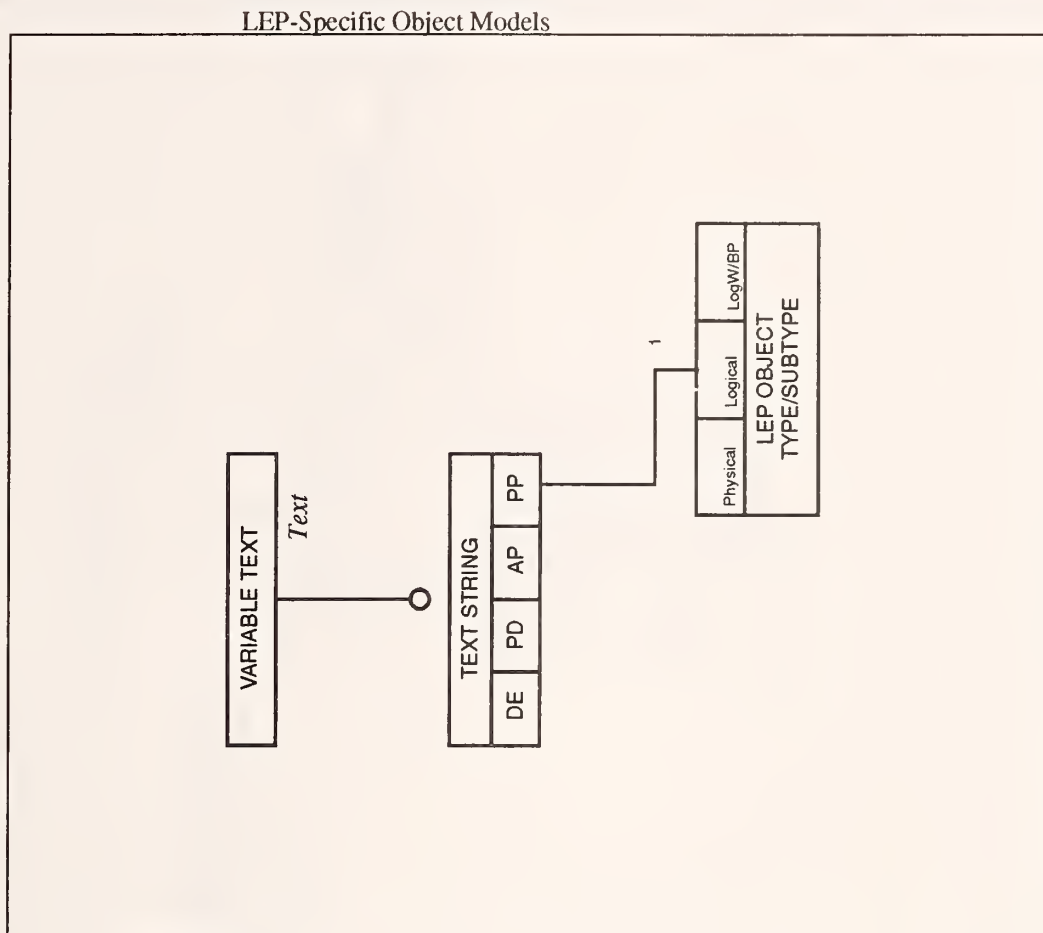
The Variable Text object must exist in a definition entity. An exception to this rule is when it is used in a Net object to display the Net name. The Object Type/Sub-Type property is used to specify which field in the parent is being displayed.

The string value, when part of a definition, is either blank or set to some default value (i.e. \$part\_number, \$value, etc.). Upon instantiation, the appropriate field value is formatted and placed in the string value of the Variable Text.

The field value, that is displayed by the Variable Text, can come from either the parent object's parameter data, a property, or an attribute that is referenced from the parent object.

#### Output:

#### Input:



### 5.3.2.54 Via

#### Description:

The Via object represent a special type of Join. It is used to electrically connect conductive material between the physical layers of the LEP.

#### Requirements/Restrictions:

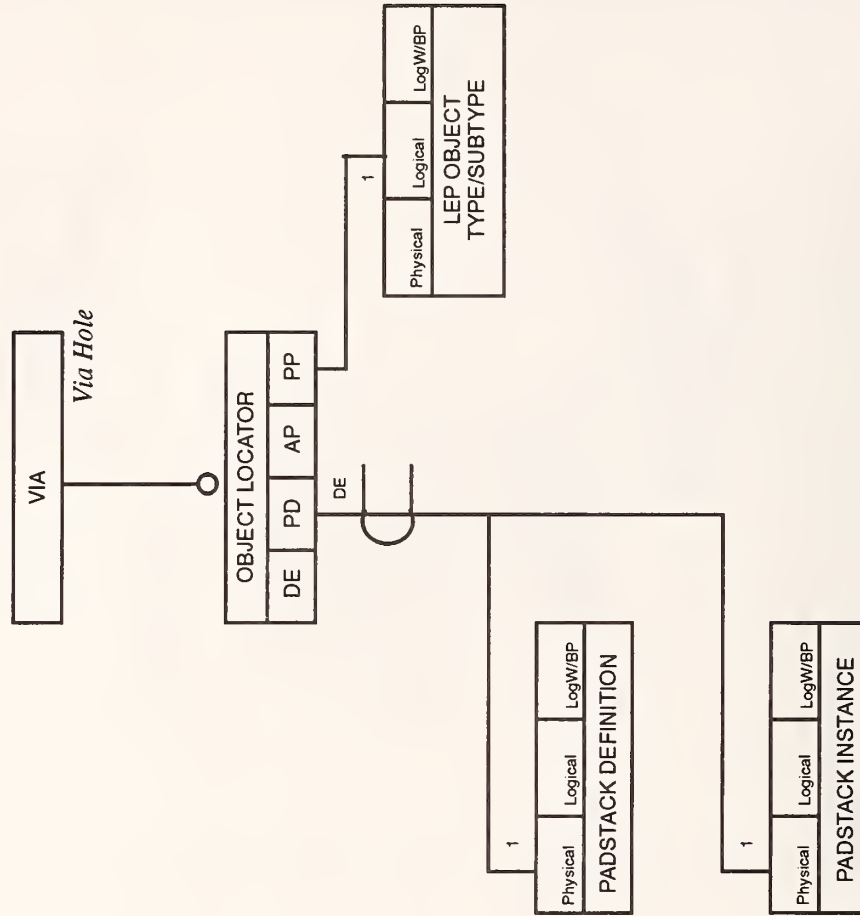
4. The LEP Object Type/Sub-Type property, which is referenced from the Object Locator object, must specify (*otype=Join, stype=Via*).
5. If the Via is subordinate to a definition that is intended to be instantiated on the LEP (i.e., Package Symbol Definition), it should reference a Padstack Definition. If the Via is subordinate to a LEP Definition, it should reference a Padstack Instance.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



5.3.2.55 Via Keepout

Description:

The Via Keepout object is a closed curve, which represents an outline in which no Vias are allowed.

Requirements/Restrictions:

Translation Usage Notes:

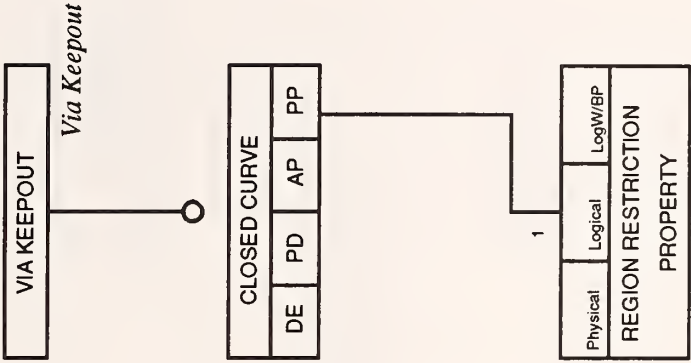
General:

The values for the Region Restriction Property should be as follows;

- VR=2
- CR=0
- TR=0
- RR=0

Output:

Input:



### 5.3.2.56 Wire Bond

**Description:**

The Wire Bond object is a special type of Join. It is used to electrically connect a pre-packaged IC or HMA to the surface of a MCM. A Wire Bond is typically soldered to a special type of Padstack (wire bond pad).

**Requirements/Restrictions:**

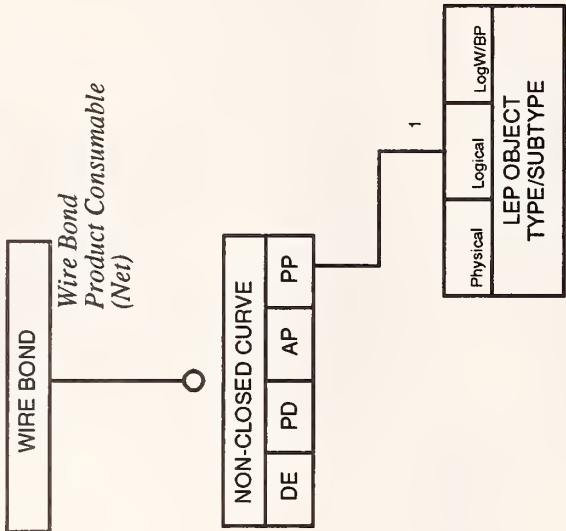
- 4. The LEP Object Type/Sub-Type property, which is referenced from the Non-Closed Curve object, must specify (*otype*=Join, *stype*=Wire\_Bond).
- 5. The wire diameter of the Wire Bond is specified through the use of the Line Width Definition object.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



## 5.3.3 Display Geometry Object Models

### 5.3.3.1 Arc

#### Description:

The Arc object represents a non-closed circular arc.

#### Requirements/Restrictions:

1. The start and end point of the IGES Circular Arc entity must not be coincident (with respect to the Global Section Minimum User-Intended Resolution).

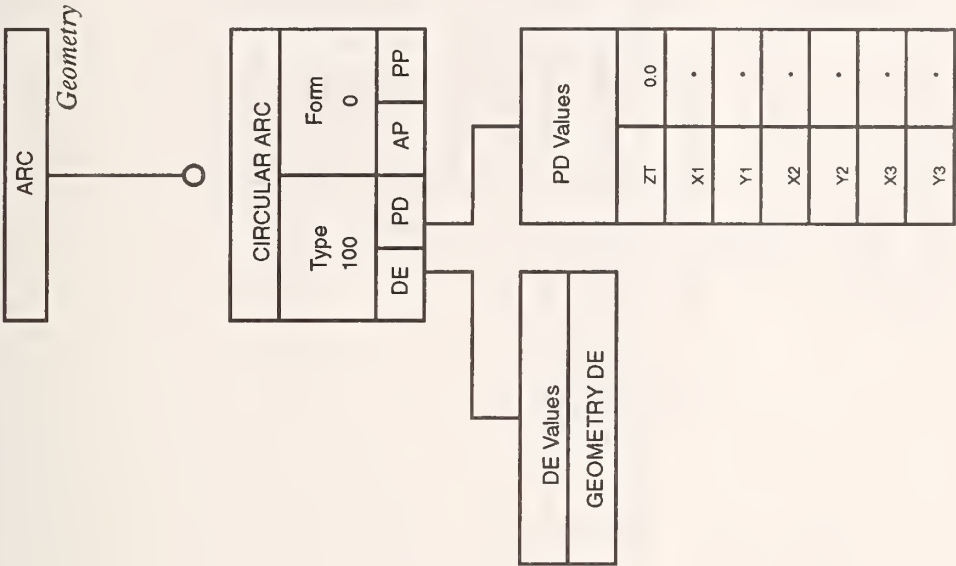
107

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.2 Circle

**Description:**

The Circle object represents a closed circular arc.

**Requirements/Restrictions:**

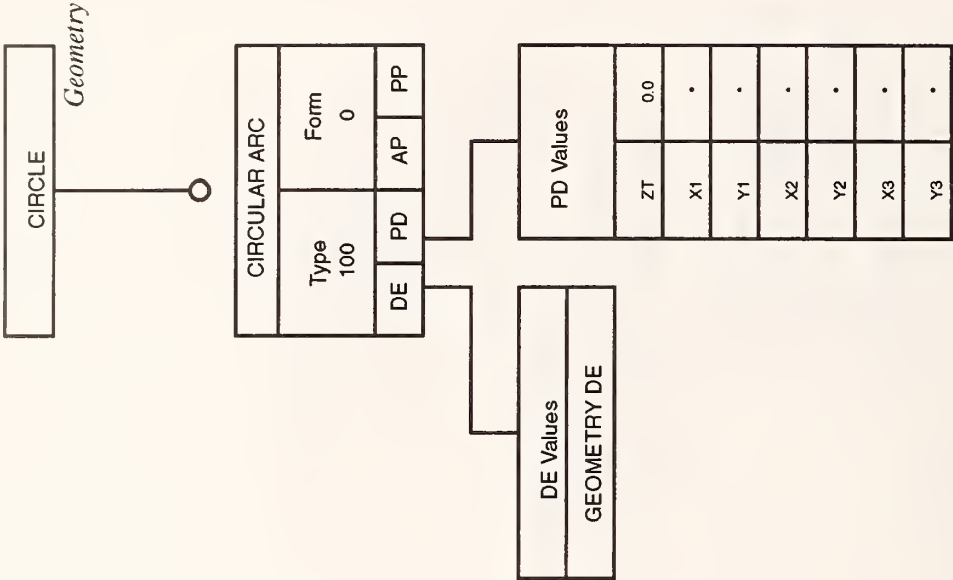
- 1. The start and end point of the IGES Circular Arc entity must be coincident (with respect to the Global Section Minimum User-Intended Resolution).

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.3.3 Closed Curve

#### Description:

1. The Closed Curve object is any one of the predefined curves which is capable of defining a closed curve. A closed curve must not self intersect or become tangent with itself at any point other than the start and end point.

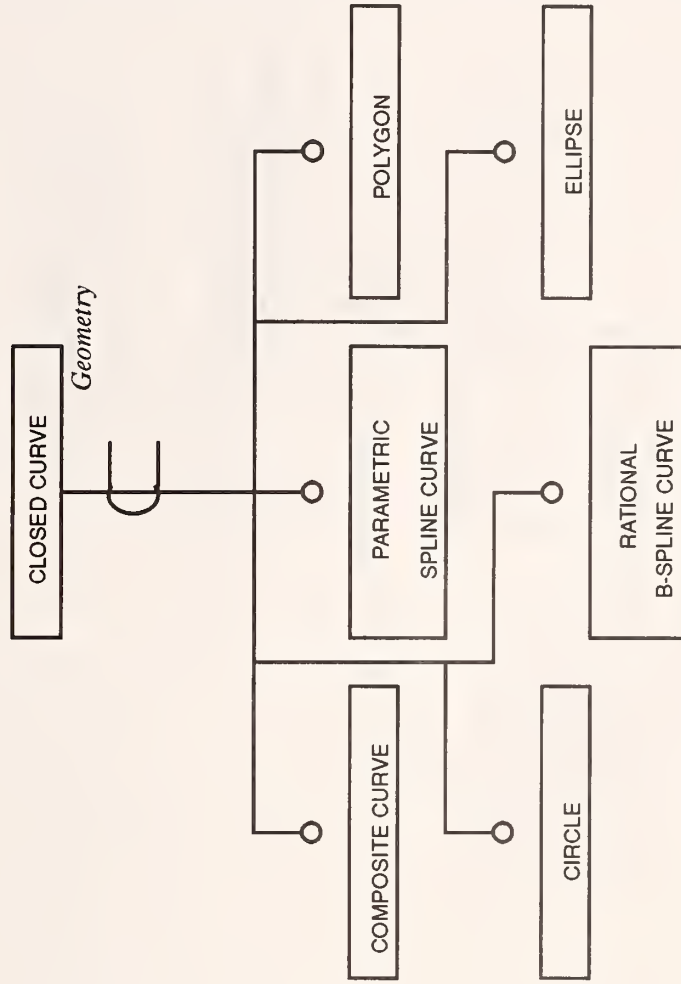
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.4 Composite Curve

**Description:**

The Composite Curve object is a contiguous curve made up of a set of two or more subordinate curves.

**Requirements/Restrictions:**

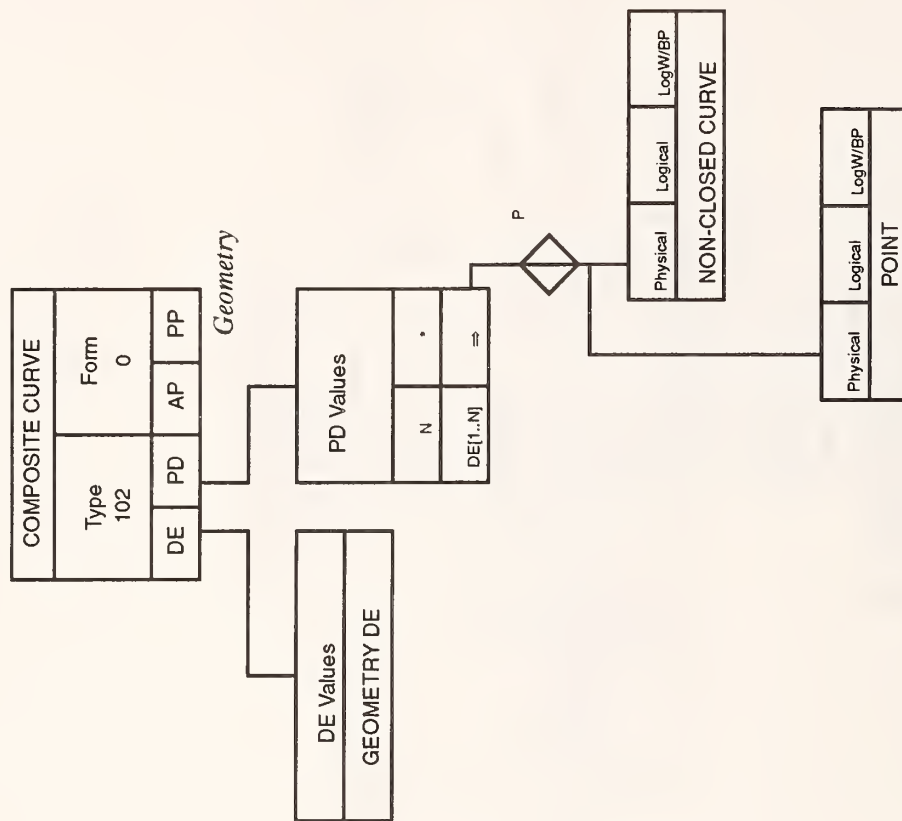
1. There must be two or more subordinate curves.
2. The Composite Curve cannot reference another Composite Curve as a subordinate entity.
3. The Composite Curve may or may not be closed.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.3.5 Curve

#### Description:

The Curve object is either a Closed Curve or a Non-Closed Curve.

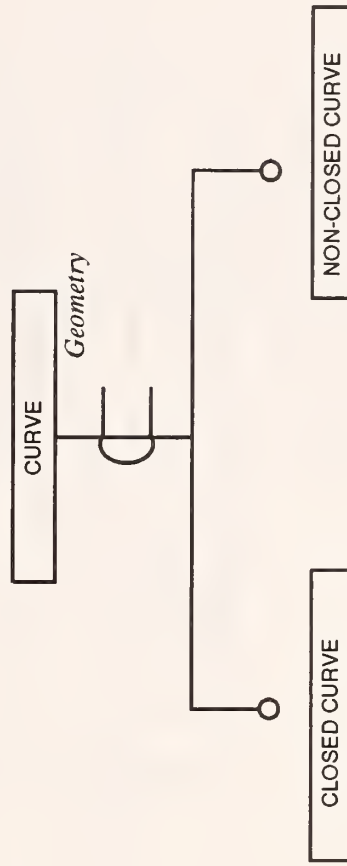
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.6 Display Geometry

**Description:**

The Display Geometry object is any one of the objects from the set of display geometry objects.

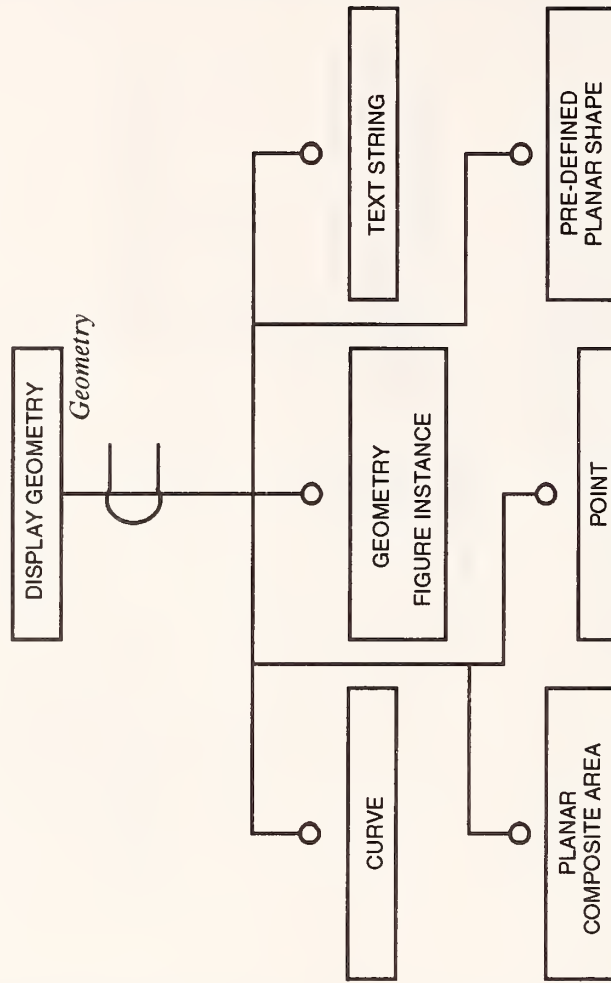
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



5.3.3.7 Ellipse

Description:

The Ellipse object represents a closed elliptical arc.

Requirements/Restrictions:

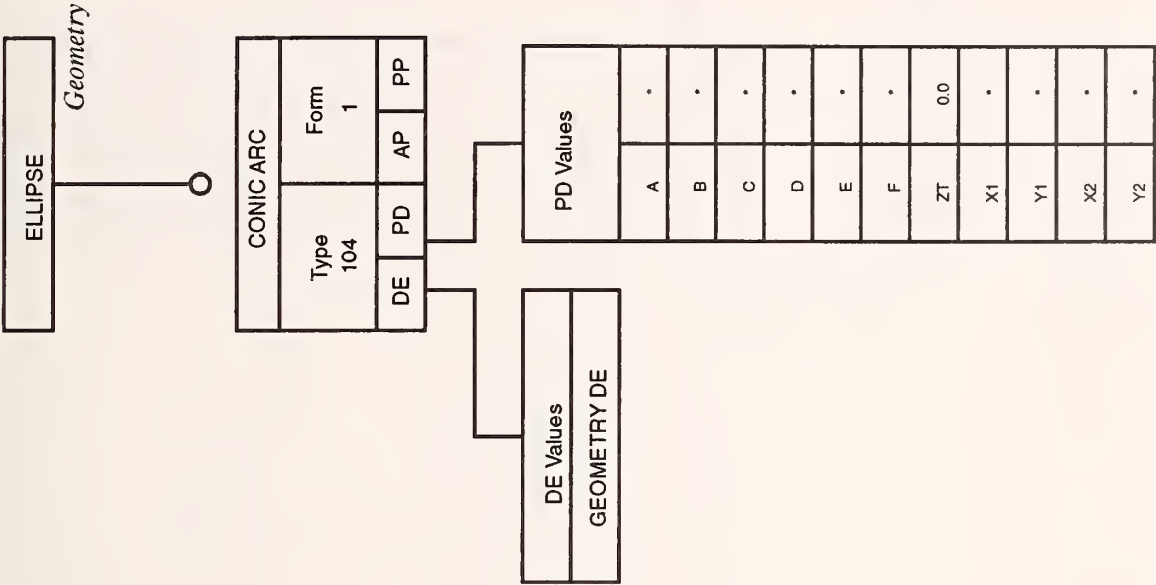
- 1. The start and end point of the IGES Conic Arc entity must be coincident (with respect to the Global Section Minimum User-Intended Resolution).

Translation Usage Notes:

General:

Output:

Input:



### 5.3.3.8 Elliptical Arc

#### Description:

The Elliptical Arc object represents a non-closed elliptical arc.

#### Requirements/Restrictions:

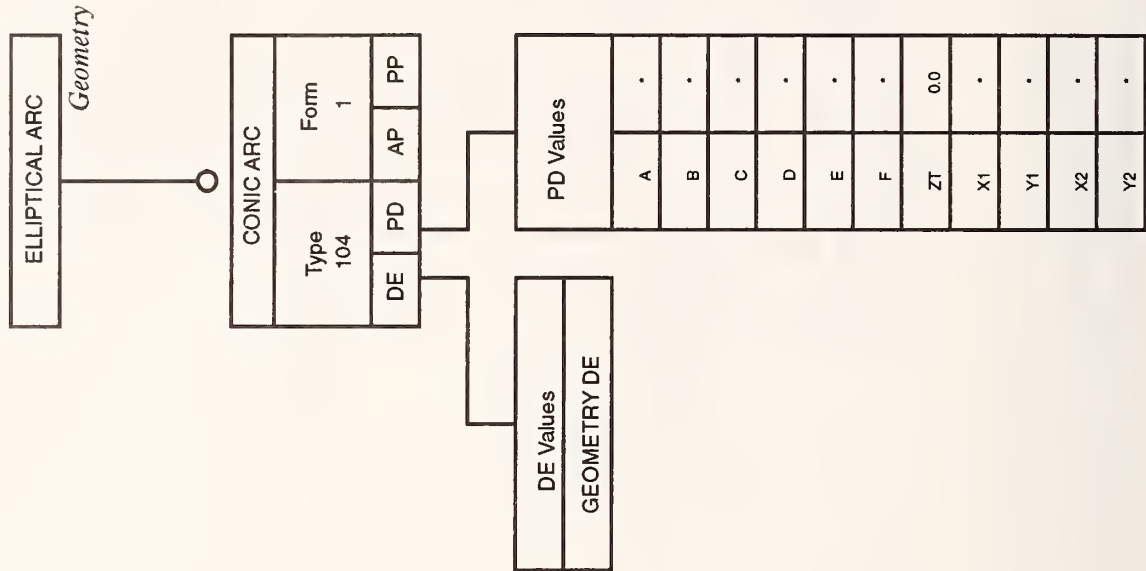
1. The start and end point of the IGES Conic Arc entity must not be coincident (with respect to the Global Section Minimum User-Intended Resolution).

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.3.9 Geometry Figure Definition

#### Description:

The Geometry Figure Definition object is a Subfigure Definition, which contains only graphic display geometry objects.

#### Requirements/Restrictions:

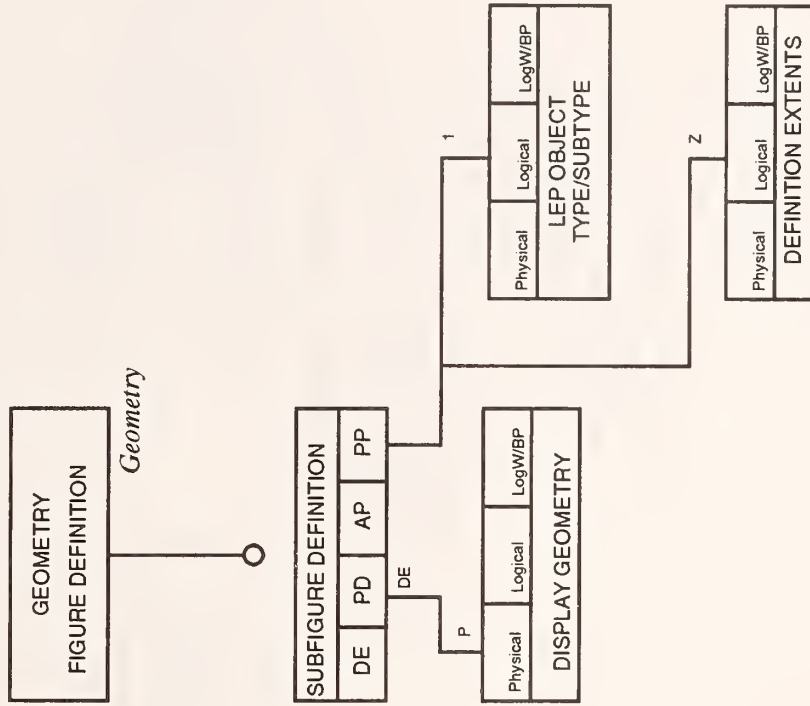
1. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Definition object, must specify (*otype=Geometry\_Figure, stype=\**).
2. The NAME field in the Subfigure Definition must be unique (for all Geometry Figure Definitions) within the scope of the IGES File.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.10 Geometry Figure Instance

#### Description:

The Geometry Figure Instance Object is either a Simple Geometry Figure Instance or a Modified Geometry Figure Instance.

#### Requirements/Restrictions:

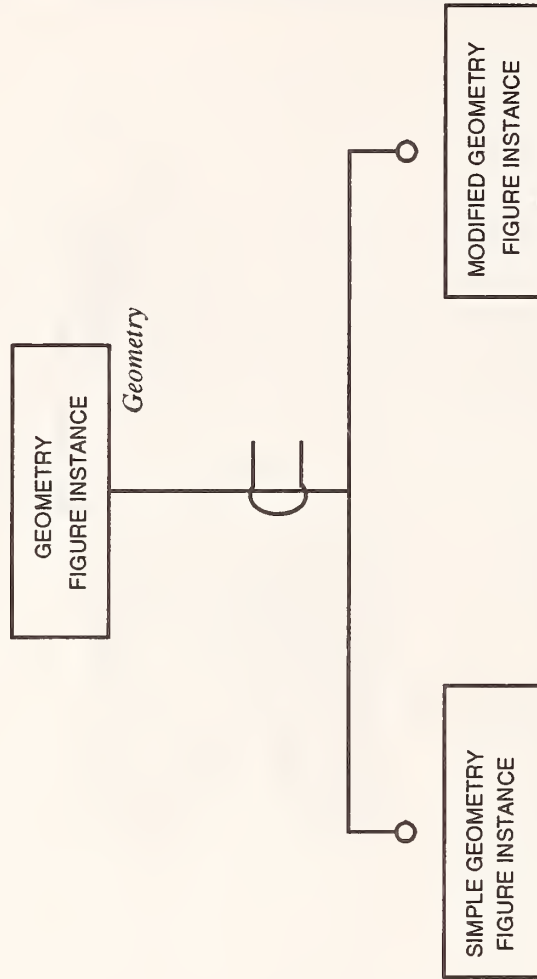
1. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (*otype*=Geometry\_Figure, *stype*=\*).

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



5.3.3.11 Hyperbolic Arc

Description:

The Hyperbolic Arc object represents a portion of a hyperbolic arc.

Requirements/Restrictions:

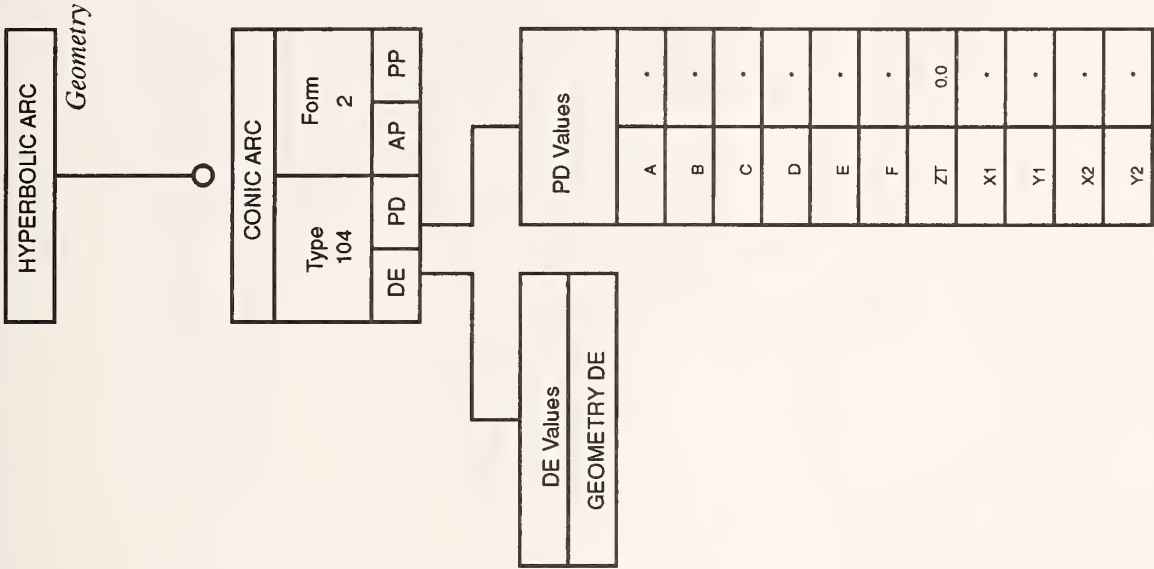
- 1. The start and end point of the IGES Conic Arc entity must not be coincident (with respect to the Global Section Minimum User-Intended Resolution).

Translation Usage Notes:

General:

Output:

Input:



### 5.3.3.12 Line

#### Description:

The Line object represents a line segment.

#### Requirements/Restrictions:

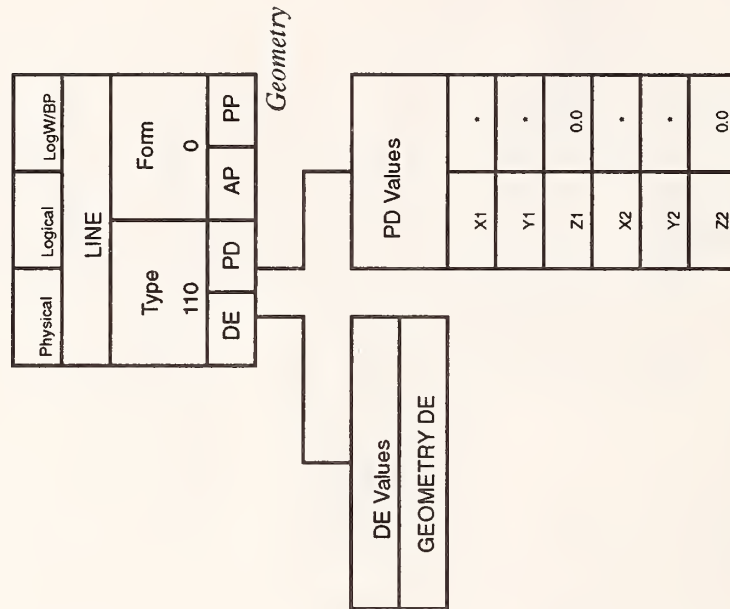
1. The start and end point of the IGES Line entity must not be coincident (with respect to the Global Section Minimum User-Intended Resolution).

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.13 Modified Geometry Figure Instance

#### Description:

The Modified Geometry Figure Instance object is a modified version of an instantiated Geometry Figure Definition.

#### Requirements/Restrictions:

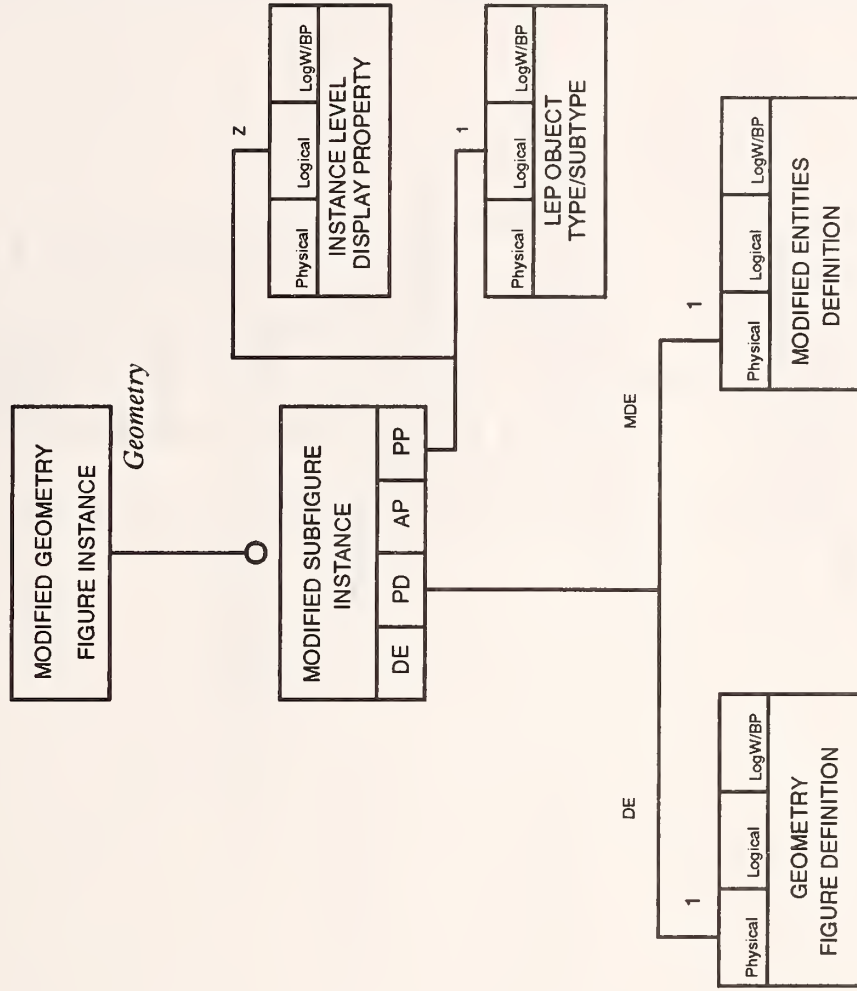
1. The LEP Object Type/Sub-Type property, which is referenced from the Modified Subfigure Instance object, must specify (*otype*=Geometry\_Figure, *stype*=\*).

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.14 Multi-Line

**Description:**

The Multi-Line object represents two or more points connected by a series of line segments.

**Requirements/Restrictions:**

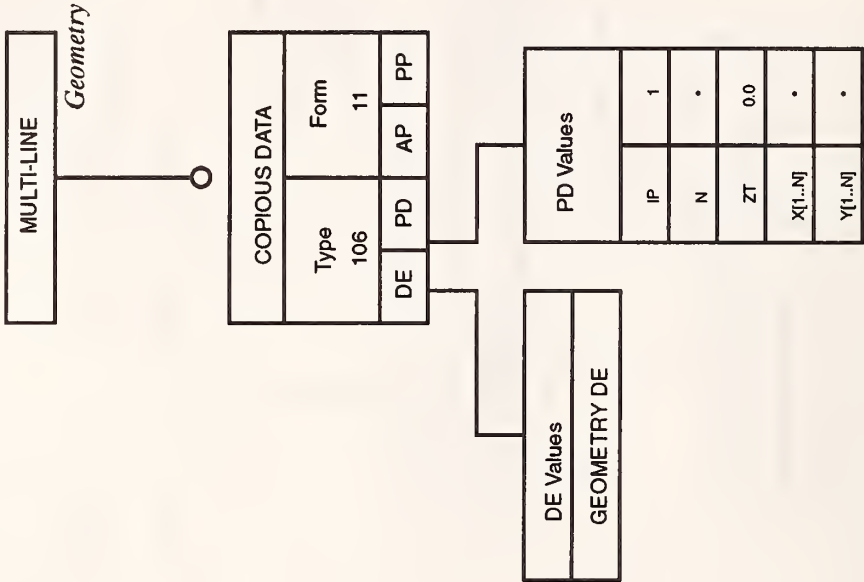
- 1. The Multi-Line may or may not be closed.
- 2. The Multi-Line must contain at least two points.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.3.15 Non-Closed Curve

#### Description:

The Non-Closed Curve object is any one of the pre-defined curve types (i.e., Line, Circular Arc, Polygon, Composite Curve, etc.) which is not closed.

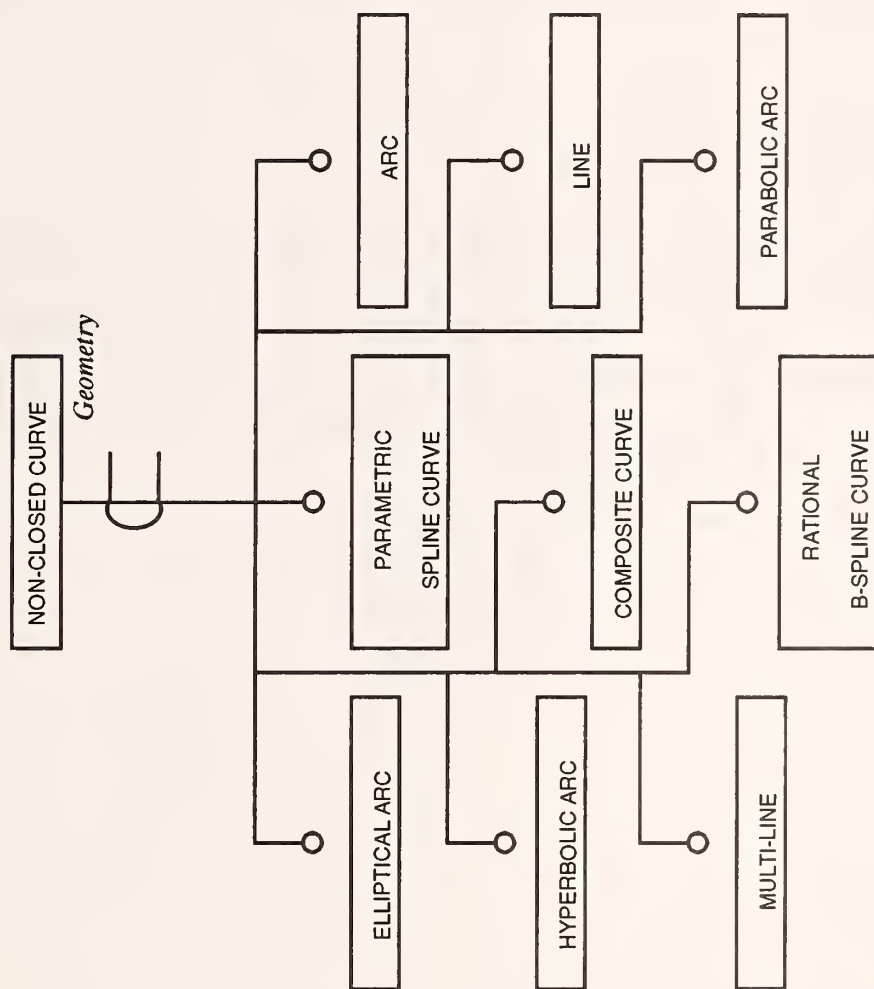
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.3.16 Parabolic Arc

**Description:**

The Parabolic Arc object is a portion of a parabolic arc.

**Requirements/Restrictions:**

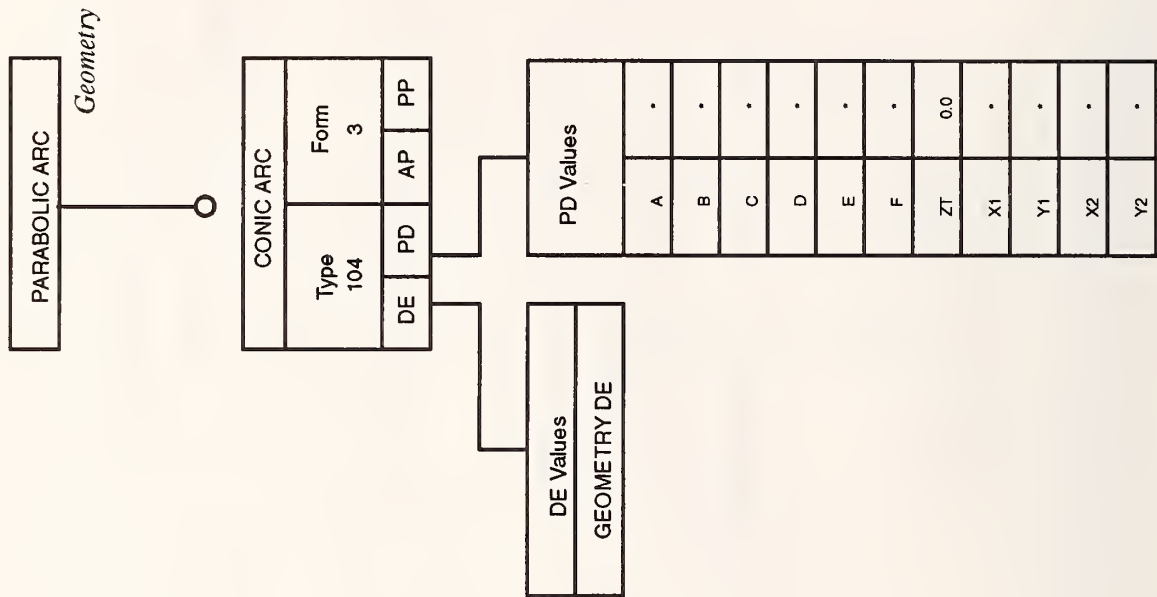
- 1. The start and end point of the IGES Conic Arc entity must not be coincident (with respect to the Global Section Minimum User-Intended Resolution).

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



5.3.3.17 Parametric Spline Curve

Description:

The Parametric Spline Curve object is a linear, quadratic, cubic, wilson fowler, modified wilson fowler, or B-spline curve.

Requirements/Restrictions:

- 1. The Parametric Spline Curve may or may not be closed.

Translation Usage Notes:

General:

Output:

Input:

PARAMETRIC SPLINE CURVE			
Type		Form	
112		0	
DE	PD	AP	PP

Geometry

DE Values
GEOMETRY DE

PD Values	
CTYPE	.
H	.
NDIM	2
N	.
T1..(N+1)	.
Ax(1)..(N+1)	.
Bx(1)..(N+1)	.
Cx(1)..(N+1)	.
Dx(1)..(N+1)	.
Ay(1)..(N+1)	.
By(1)..(N+1)	.
Cy(1)..(N+1)	.
Dy(1)..(N+1)	.
Az(1)..(N+1)	.

Bz(1)..(N+1)	.
Cz(1)..(N+1)	.
Dz(1)..(N+1)	.
TPX0	.
TPX1	.
TPX2	.
TPX3	.
TYP0	.
TYP1	.
TYP2	.
TYP3	.
TPZ0	.
TPZ1	.
TPZ2	.
TPZ3	.

### 5.3.3.18 Planar Composite Area

**Description:**

The Planar Composite Area object represents a single closed boundary curve, which has, one or more closed internal island curves.

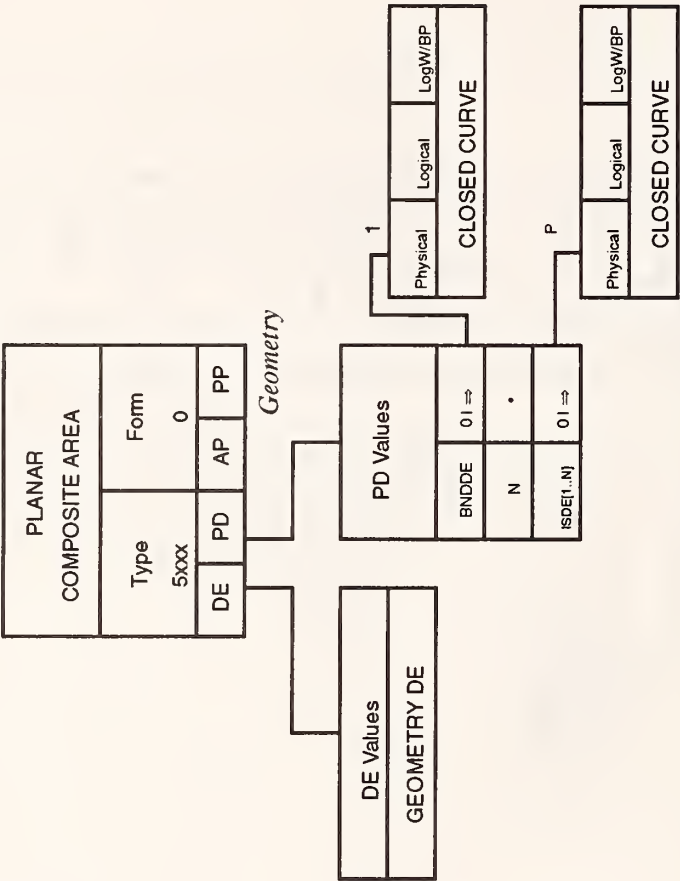
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



5.3.3.19 Polygon

Description:

The Polygon object is a closed multi-line that does not self intersect or become tangent with itself at any point, other than the start and end point.

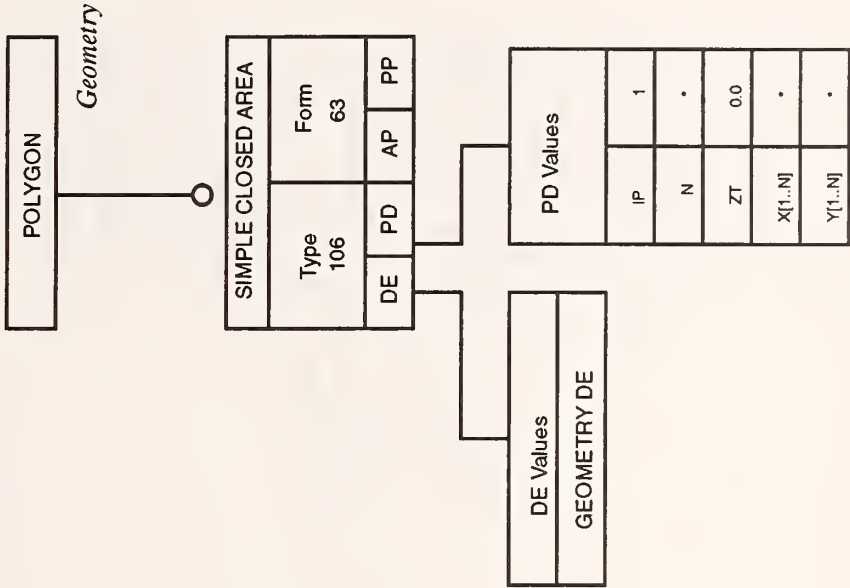
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



5.3.3.20 Point

Description:

The Point object represents a 2-D geometric construction point.

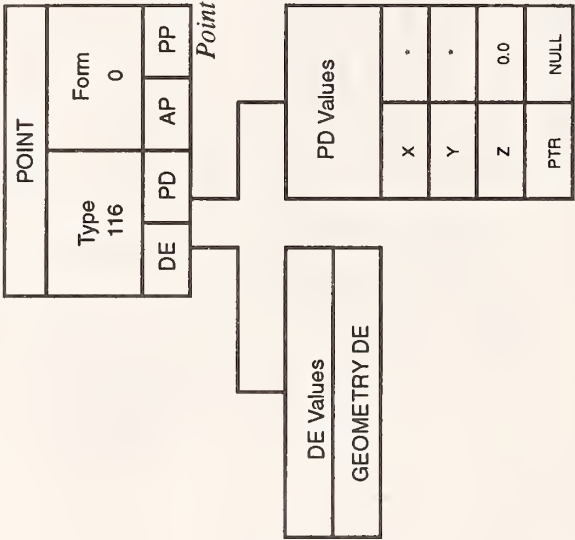
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



5.3.3.21 Predefined Planar Shape

Description:

The Predefined Planar Shape object is a closed curve, which represents one of a set of predefined shapes, where the specific shape is defined by three floating point parameters.

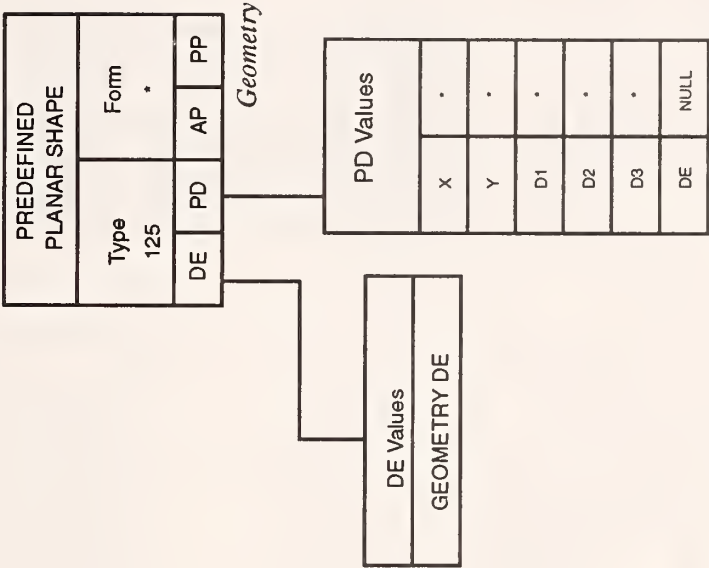
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.3.22 Rational B-Spline Curve

**Description:**

The Rational B-Spline Curve object represents either a parametric, linear, circular, elliptical, parabolic, or hyperbolic curve, which is defined by a series of knots and corresponding weights.

**Requirements/Restrictions:**

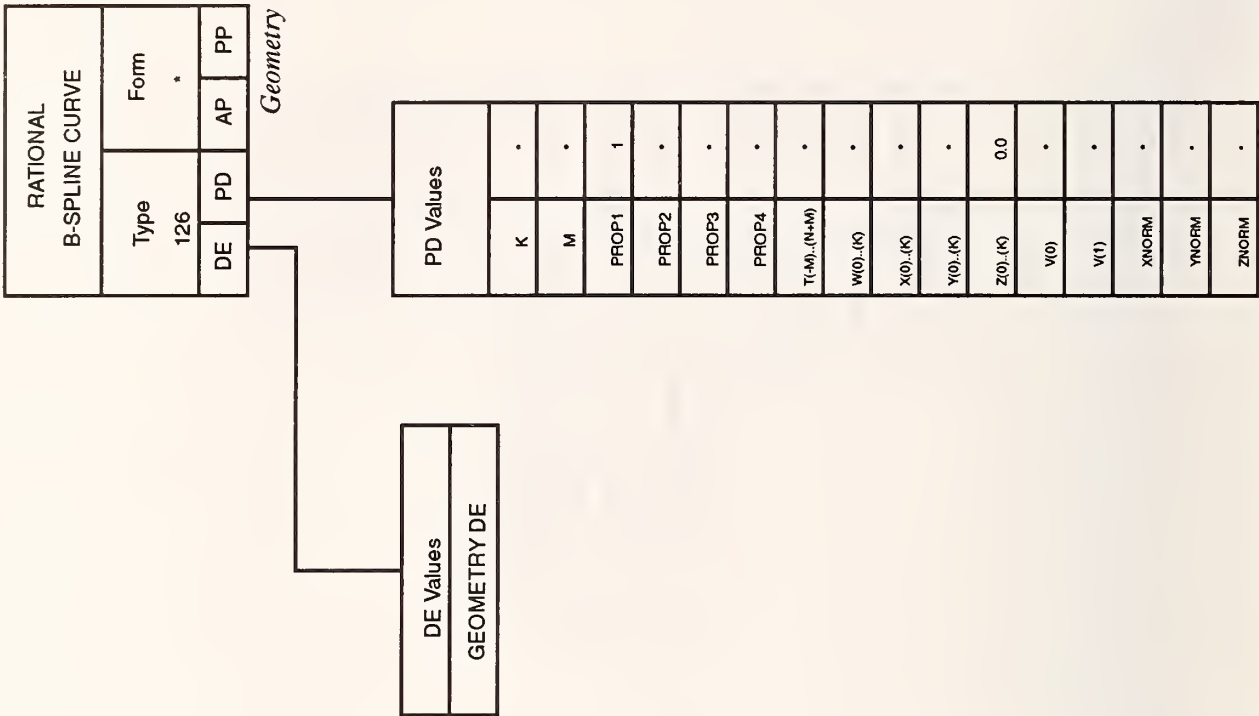
- 1. The Rational B-Spline Curve may or may not be closed.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



# 5.3.3.23 Simple Geometry Figure Instance

## Description:

The Simple Geometry Figure Instance object is an instantiated Geometry Figure ion either a Geometry Figure Instance or a Modified Geometry Figure Instance.

## Requirements/Restrictions:

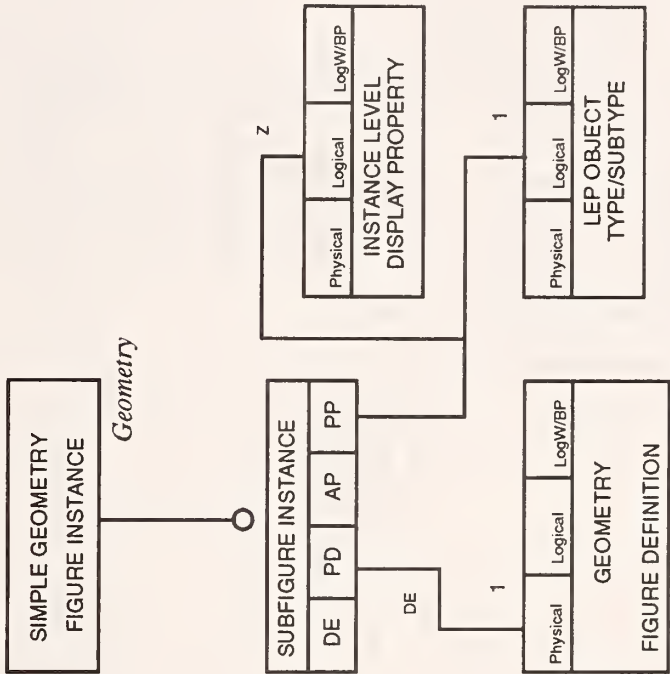
1. The LEP Object Type/Sub-Type property, which is referenced from the Subfigure Instance object, must specify (*otype*=Geometry\_Figure, *stype*=\*).

## Translation Usage Notes:

### General:

### Output:

### Input:



### 5.3.3.24 Text String

#### Description:

The Text String object is a graphic general note containing one or more related character strings.

#### Requirements/Restrictions:

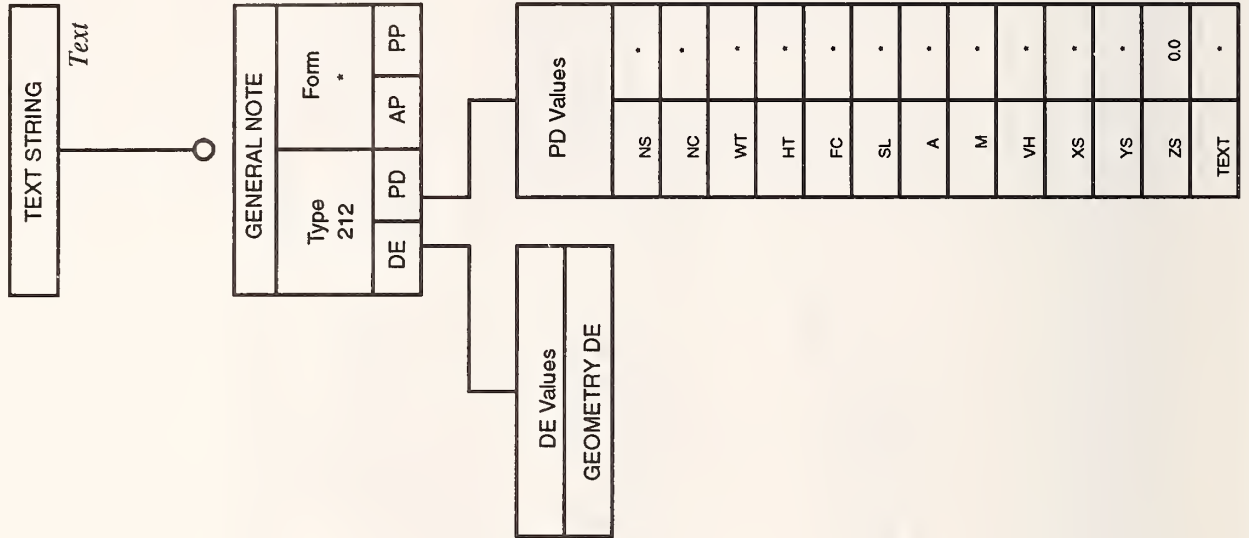
1. The General Note must be Form 0, 1, 6, 7, or 8.
2. The General Note FC field must be either 1, 1001, 1002, or 1003.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



# 5.3.4 Miscellaneous Object Models

## 5.3.4.1 Attribute Table Definition

### Description:

The Attribute Table Definition object maps directly to the IGES Attribute Table Definition entity (Type 322 Form All). Please refer to the IGES specification for additional information.

### Requirements/Restrictions:

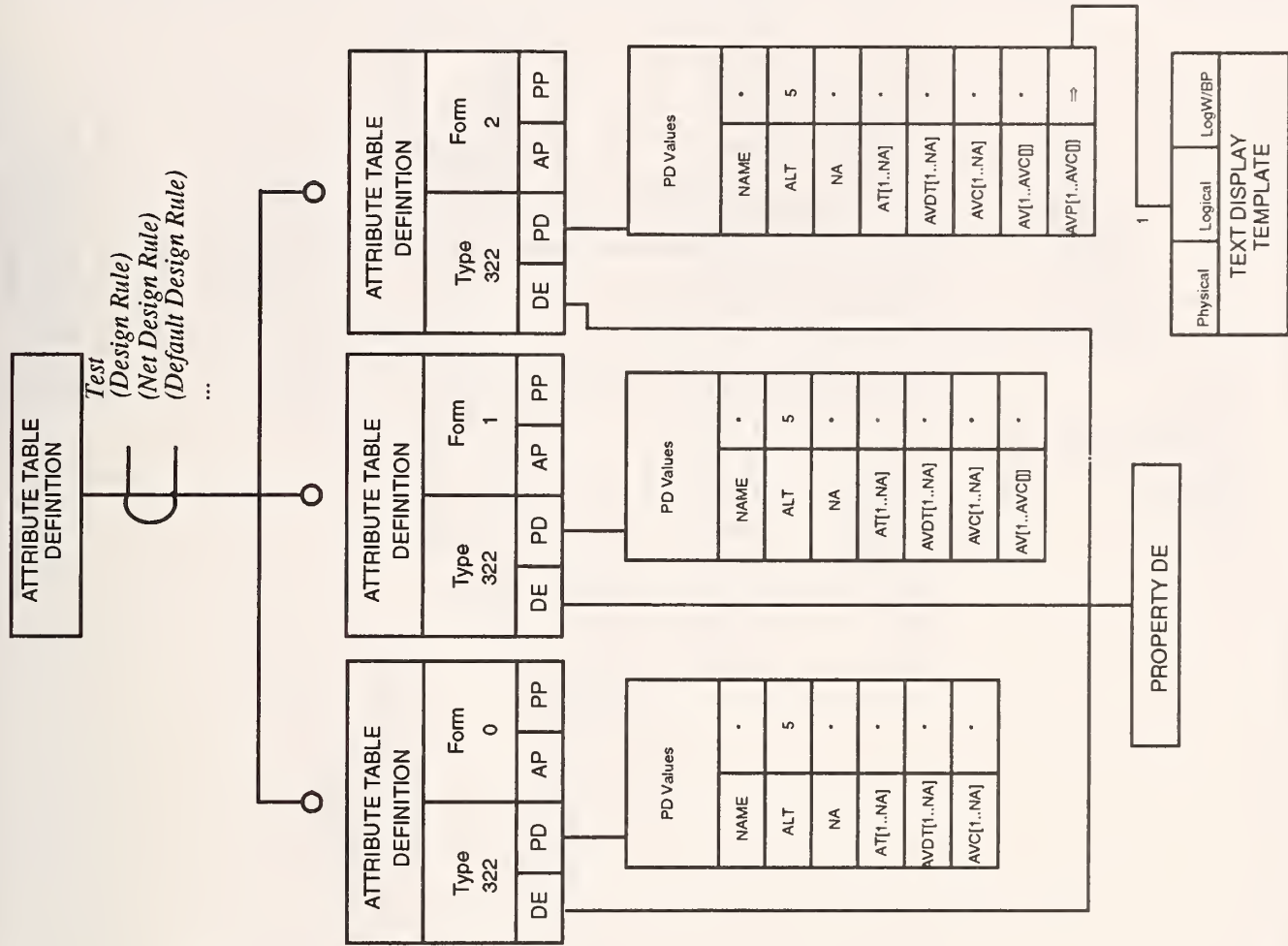
1. The Name field in the Attribute Table Definition must be unique (for all Attribute Table Definitions) within the scope of the IGES Model.

### Translation Usage Notes:

**General:**

**Output:**

**Input:**



### 5.3.4.2 Attribute Table Instance

#### Description:

The Attribute Table Instance object maps directly to the IGES Attribute Table Instance entity (Type 422 Form All). Please refer to the IGES specification for additional information.

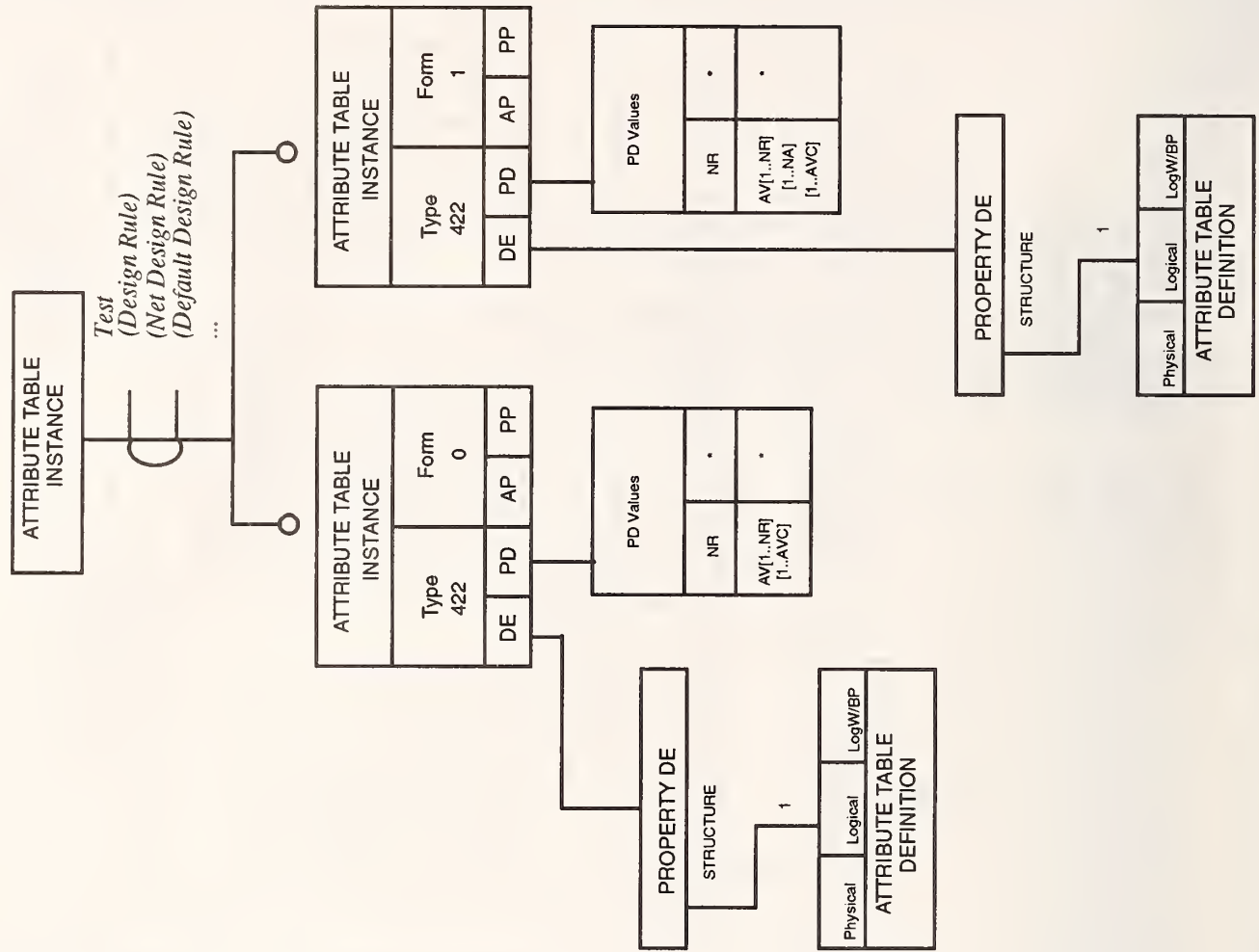
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



5.3.4.3 Definition Extents

Description:

The Definition Extents object maps directly to the IGES Definition Extents property (Type 406 Form 5xxx). Please refer to the IGES specification for additional information.

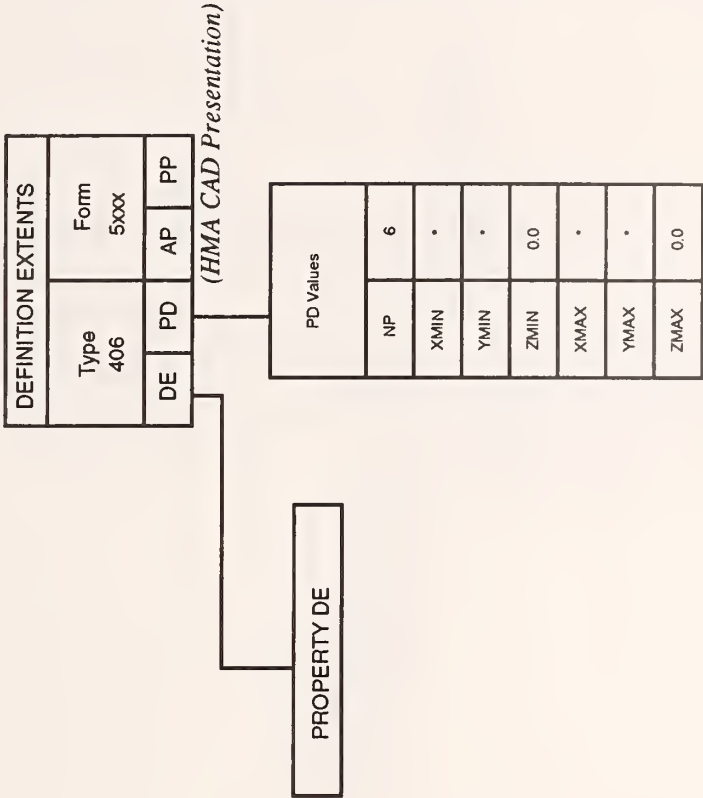
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.4.4 Generic Data Property

#### Description:

The Generic Data Property object maps directly to the IGES Generic Data Property (Type 406 Form 27). Please refer to the IGES specification for additional information.

#### Requirements/Restrictions:

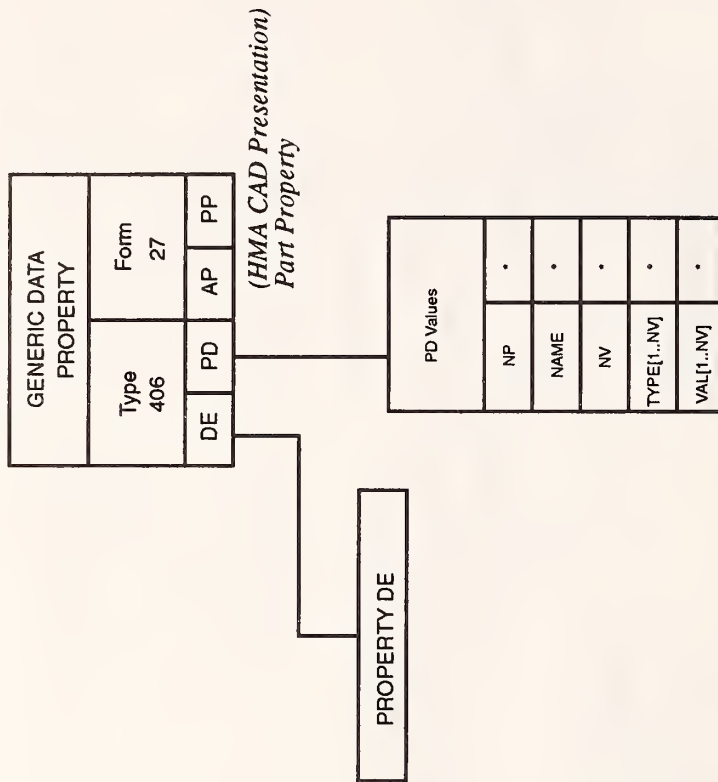
1. The Generic Data object can be referenced from the Property Pointer list of any other object in the IGES model.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.4.5 Hierarchy Property

#### Description:

The Hierarchy object maps directly to the IGES Hierarchy Property (Type 406 Form 10). Please refer to the IGES specification for additional information.

#### Requirements/Restrictions:

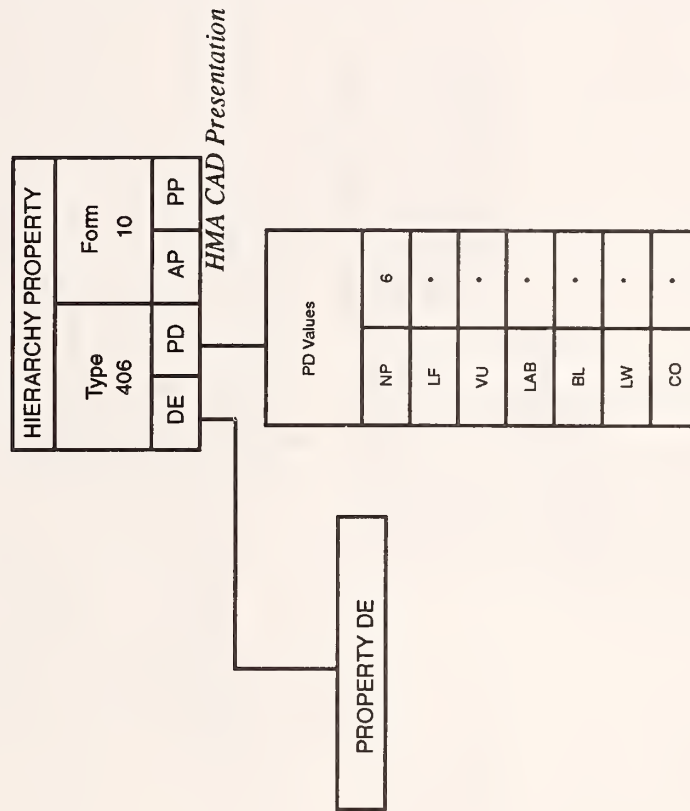
1. The Hierarchy object can be referenced from the Property Pointer list of any object that references physically subordinate children.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.4.6 Instance Level Display Property

**Description:**

The Instance Level Display Property object maps directly to the IGES Instance Level Display Property (Type 406 Form 5xxx). Please refer to the IGES specification for additional information.

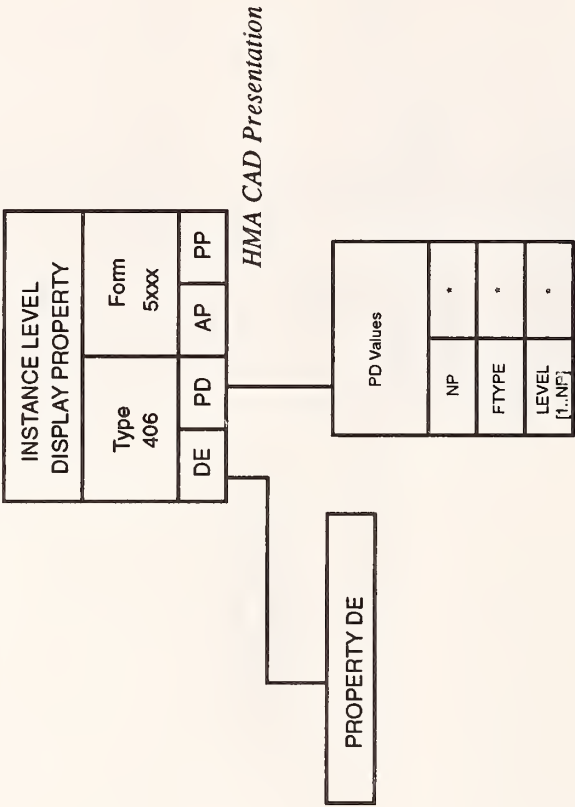
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.4.7 Modified Entities Definition

**Description:**

The Modified Entities Definition object maps directly to the IGES Modified Entities Definition (Type 5xxx Form 0). Please refer to the IGES specification for additional information.

**Requirements/Restrictions:**

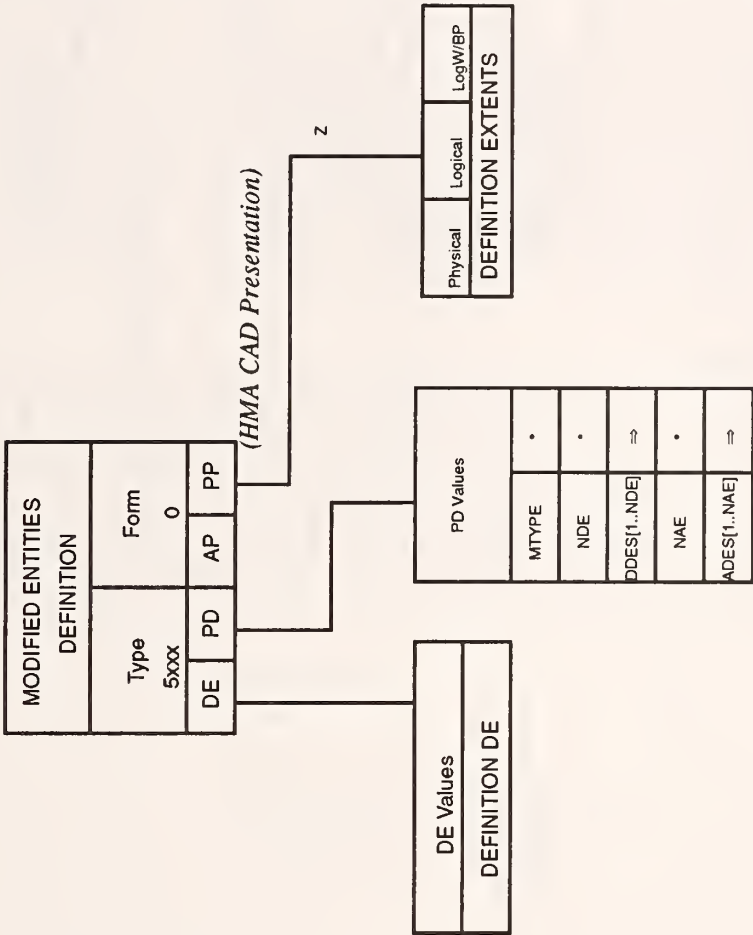
- 1. You can only add entities that are valid within the original Subfigure Definition or Network Subfigure Definition.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.4.8 Modified Network Subfigure Instance

**Description:**

The Modified Network Subfigure Instance object maps directly to the IGES Modified Network Subfigure Instance entity (Type 420 Form 1). Please refer to the IGES specification for additional information.

**Requirements/Restrictions:**

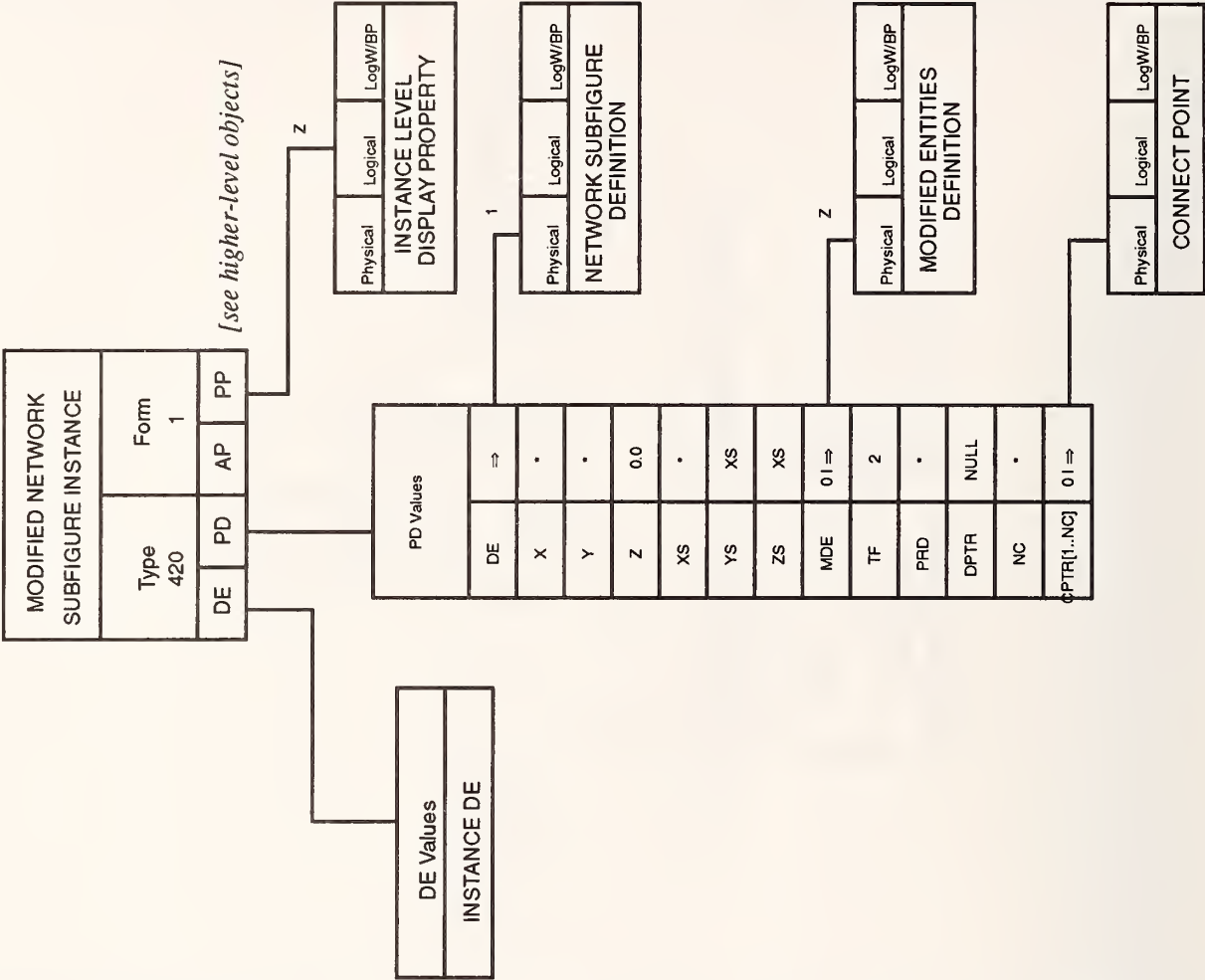
- 1. If the Modified Network Subfigure Instance has not been modified, the MDE pointer should be 0 or null.
- 2. The DPTR is not used to display the primary reference designator (PRD). The Variable Text object is used for this purpose.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.4.9 Modified Subfigure Instance

#### Description:

The Modified Subfigure Instance object maps directly to the IGES Modified Subfigure Instance entity (Type 408 Form 1). Please refer to the IGES specification for additional information.

#### Requirements/Restrictions:

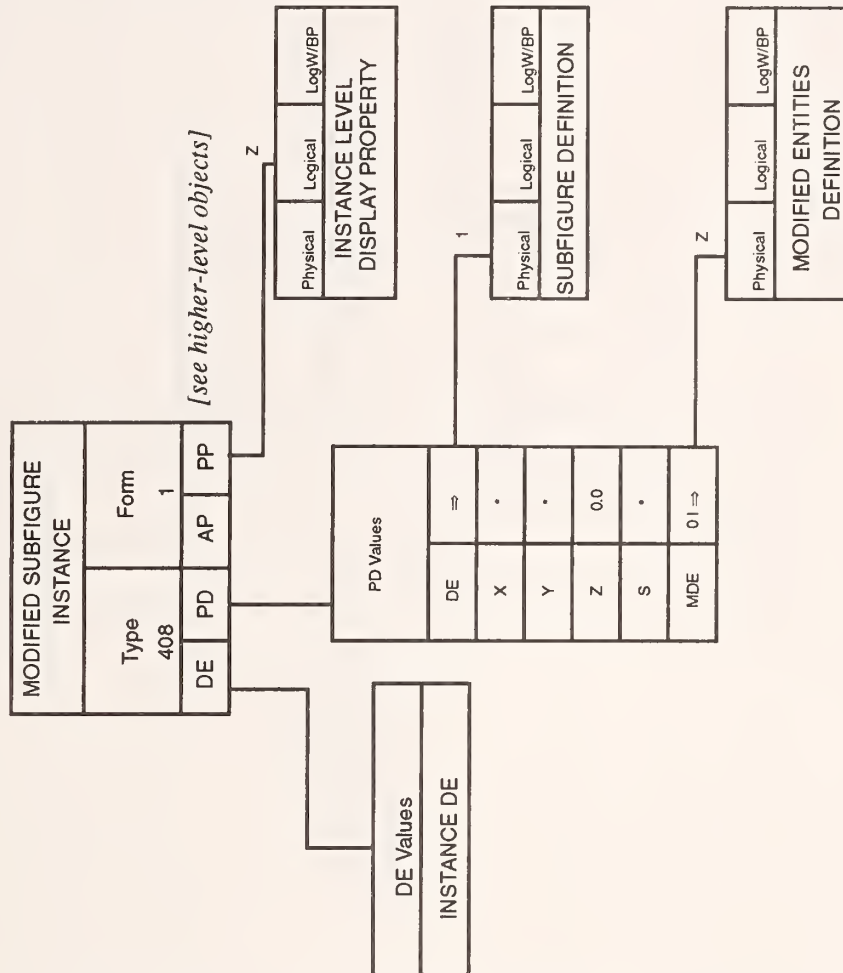
1. If the Modified Subfigure Instance has not been modified, the MDE pointer should be 0 or null.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



5.3.4.10 Name

Description:

The Name object maps directly to the IGES Name Property (Type 406 Form 15). Please refer to the IGES specification for additional information.

Requirements/Restrictions:

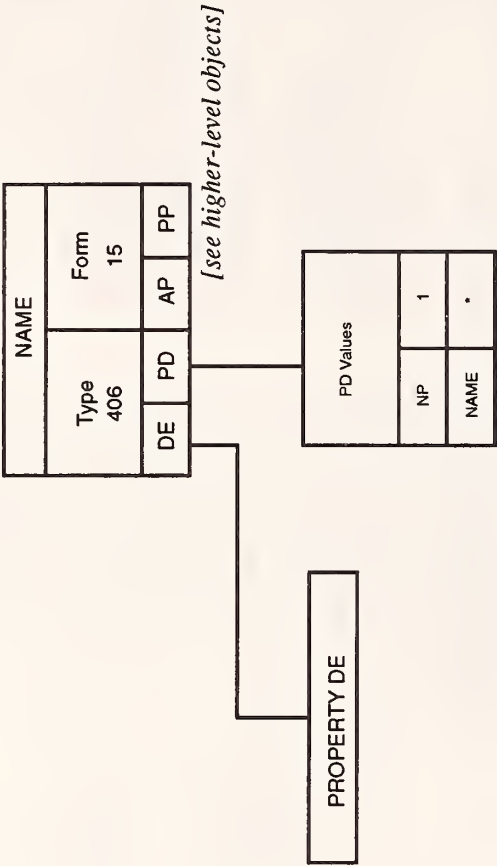
- 1. The Name object can be referenced by any other object that does not have an explicit name field in it's parameter data.

Translation Usage Notes:

General:

Output:

Input:



### 5.3.4.11 Network Subfigure Definition

**Description:**

The Network Subfigure Definition object maps directly to the IGES Network Subfigure Definition entity (Type 320 Form 0). Please refer to the IGES specification for additional information.

**Requirements/Restrictions:**

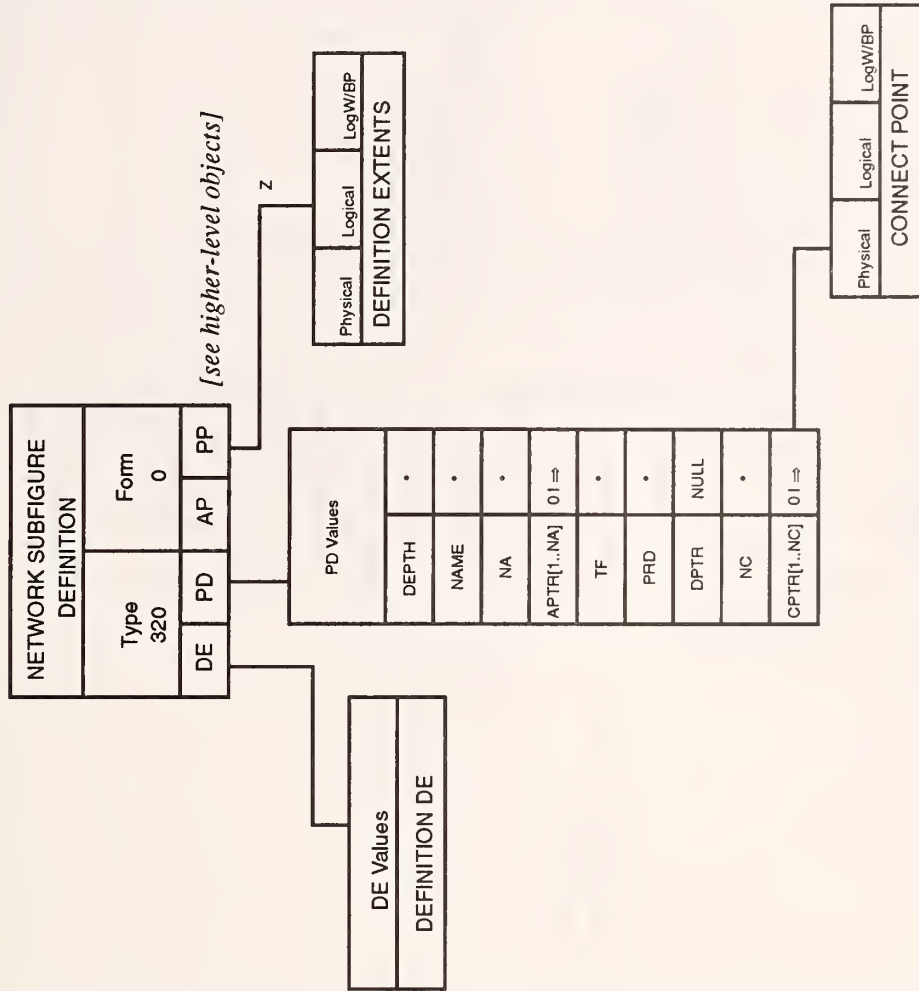
- 2. The NAME field in the Network Subfigure Definition must be unique (for all Network Subfigure Definitions of the same object type) within the scope of the IGES File.
- 3. The DPTR is not used to display the primary reference designator (PRD). The Variable Text object is used for this purpose.

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.4.12 Network Subfigure Instance

#### Description:

The Network Subfigure Instance object maps directly to the IGES Network Subfigure Instance entity (Type 420 Form 0). Please refer to the IGES specification for additional information.

#### Requirements/Restrictions:

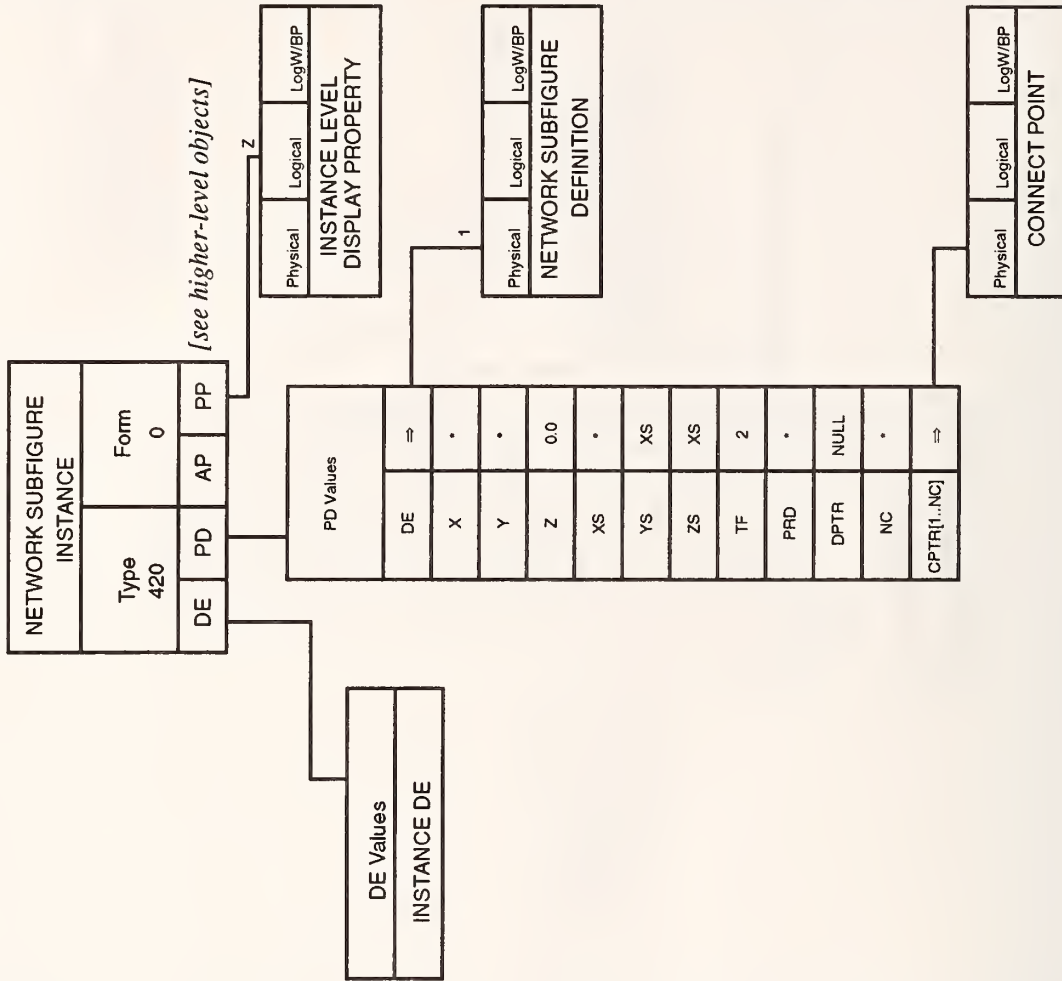
1. The DPTR is not used to display the primary reference designator (PRD). The Variable Text object is used for this purpose.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



5.3.4.13 Object Locator

Description:

The Object Locator object maps directly to the IGES Object Locator entity (Type 5xxx Form 0). Please refer to the IGES specification for additional information.

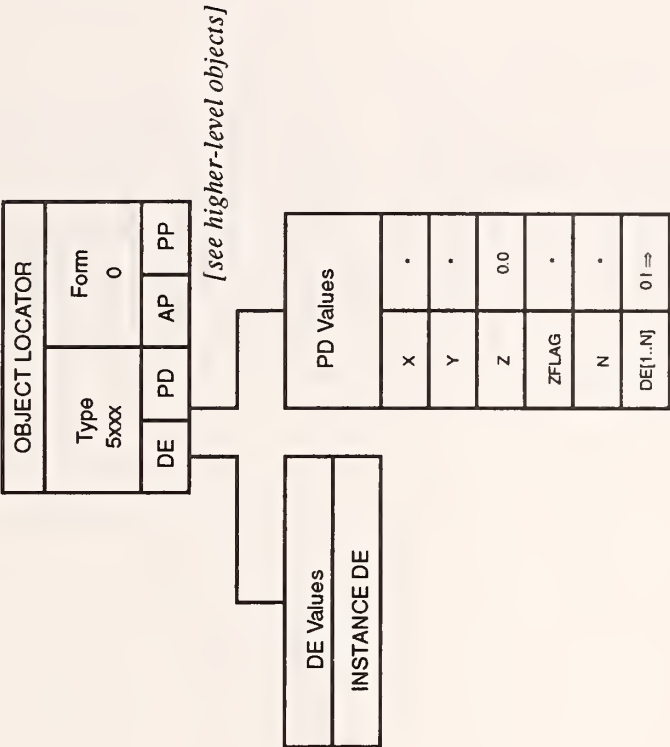
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.4.14 Part Number Property

#### Description:

The Part Number Property object maps directly to the IGES Part Number Property (Type 406 Form 9). Please refer to the IGES specification for additional information.

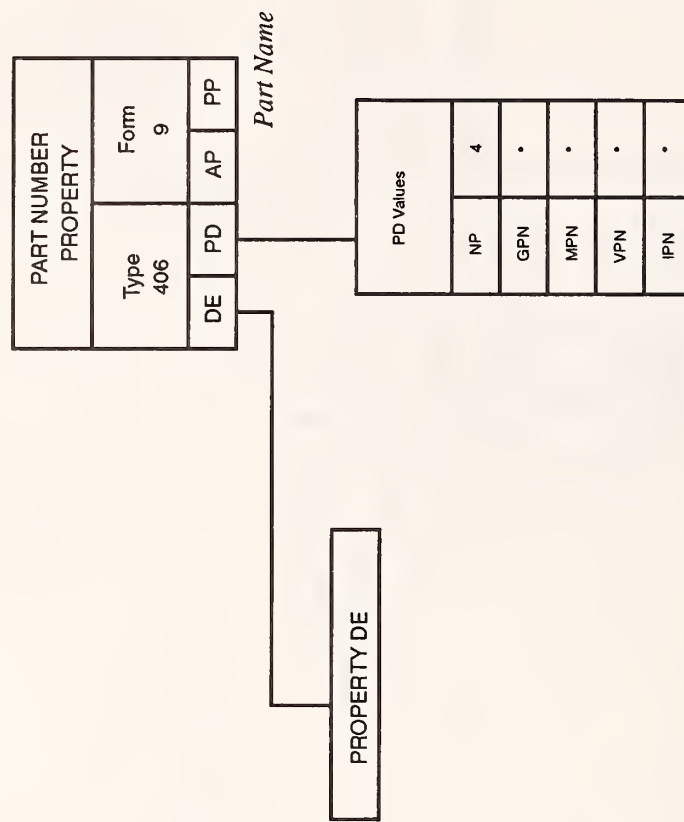
#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

144 Output:

#### Input:



### 5.3.4.15 Region Restriction

#### Description:

The Region Restriction object maps directly to the IGES Region Restriction Property (Type 406 Form 2). Please refer to the IGES specification for additional information.

#### Requirements/Restrictions:

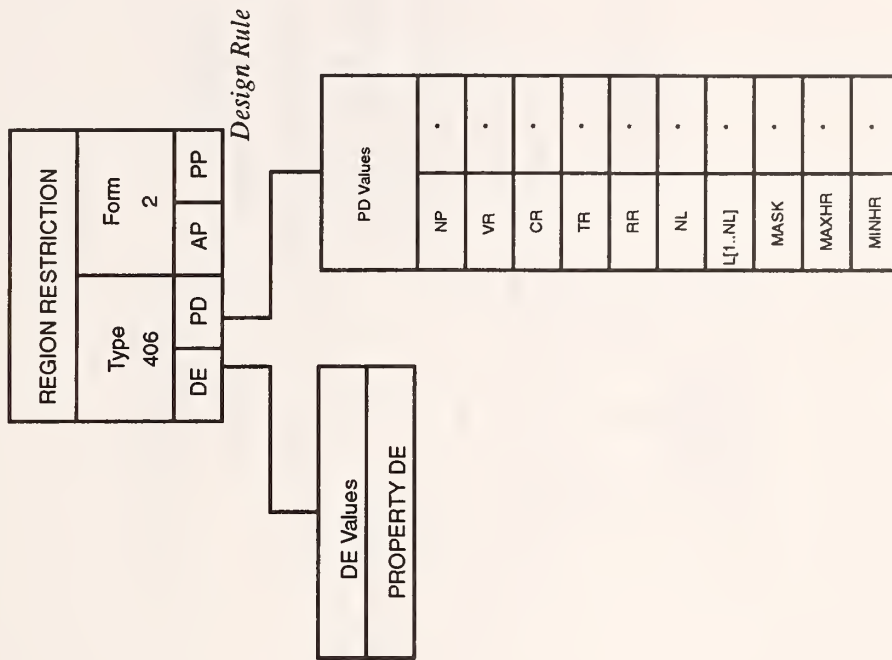
#### Translation Usage Notes:

#### General:

- 15 Utilize the DE Level attribute to specify the levels in which the restriction applies. The DE Level attribute of the base entity specifies which level(s) the base entity exists on.

#### Output:

#### Input:



### 5.3.4.16 Subfigure Definition

#### Description:

The Subfigure Definition object maps directly to the IGES Subfigure Definition entity (Type 308 Form 0). Please refer to the IGES specification for additional information.

#### Requirements/Restrictions:

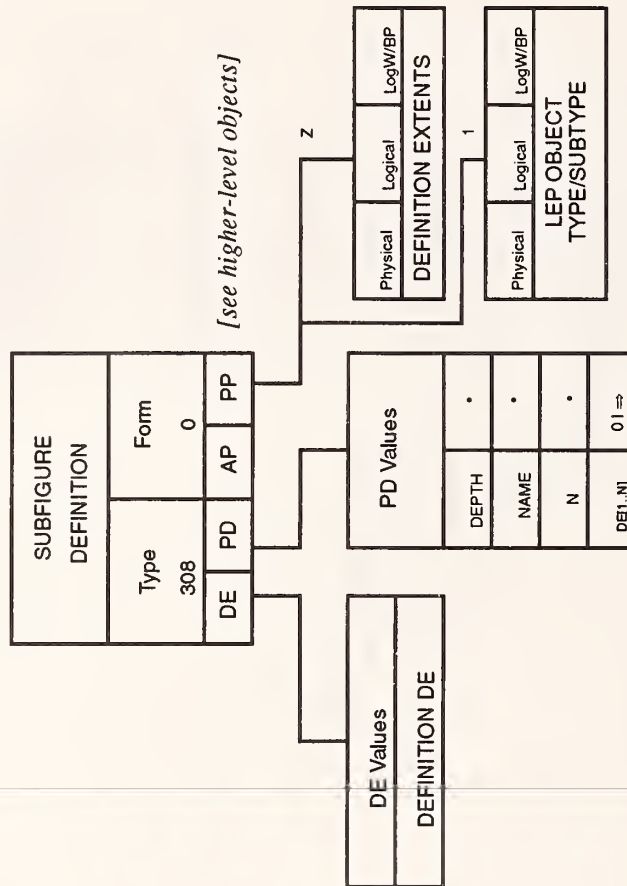
1. The NAME field in the Subfigure Definition must be unique (for all Subfigure Definitions of the same object type) within the scope of the IGES File.

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:



### 5.3.4.17 Subfigure Instance

**Description:**

The Subfigure Instance object maps directly to the IGES Subfigure Instance entity (Type 408 Form 0). Please refer to the IGES specification for additional information.

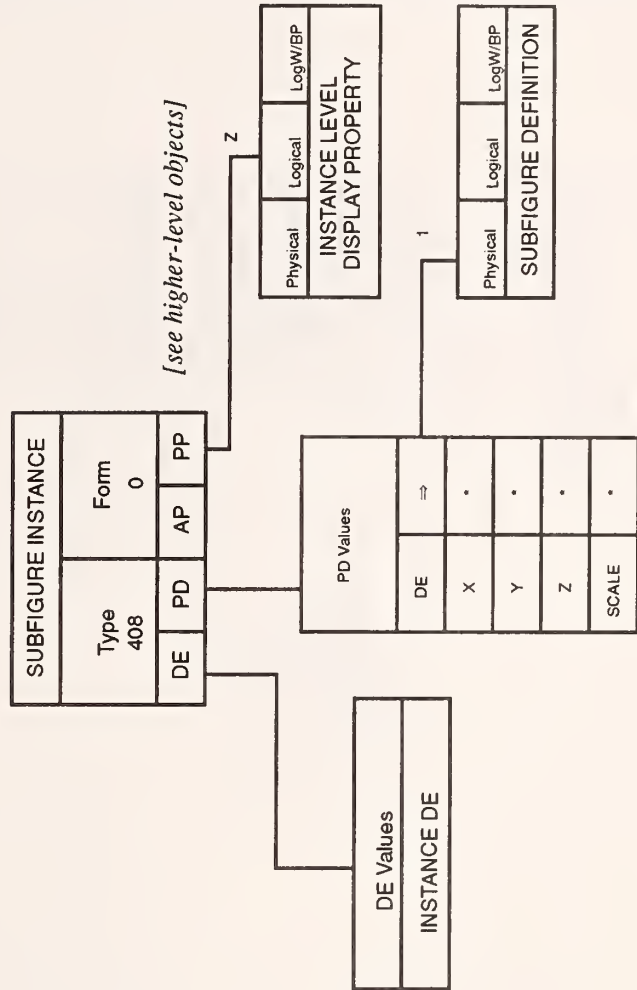
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.4.18 Text Display Template

**Description:**

The Text Display Template object maps directly to the IGES Text Display Template entity (Type 312 Form 1). Please refer to the IGES specification for additional information.

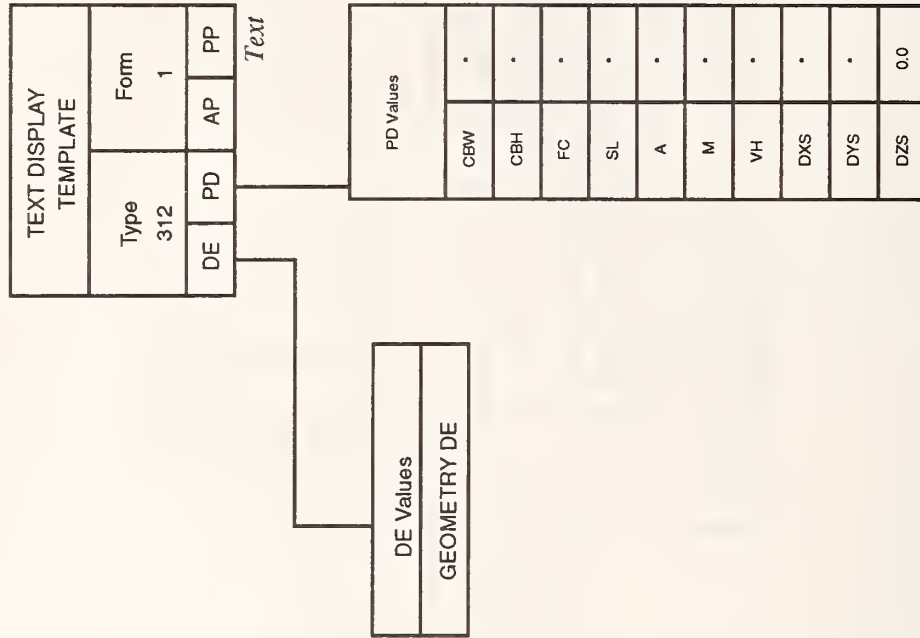
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



## 5.3.5 DE Referenced Object Models

### 5.3.5.1 Color Definition

#### Description:

The Color Definition object enables an entity to be displayed a specific color, based on a percentage of red, green and blue intensity.

#### Requirements/Restrictions:

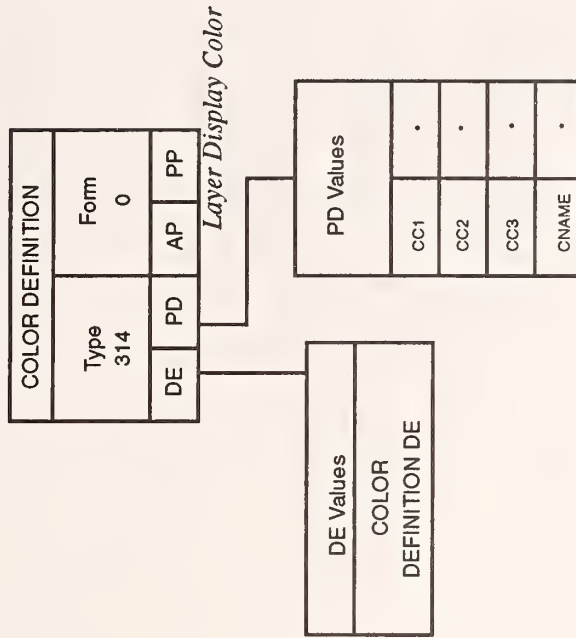
1. The CNAME field in the Color Definition must be unique (for all Color Definitions) within the scope of the IGES File.

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



### 5.3.5.2 Level Definition

**Description:**

The Level Definition object enables an entity to exist on one or more levels.

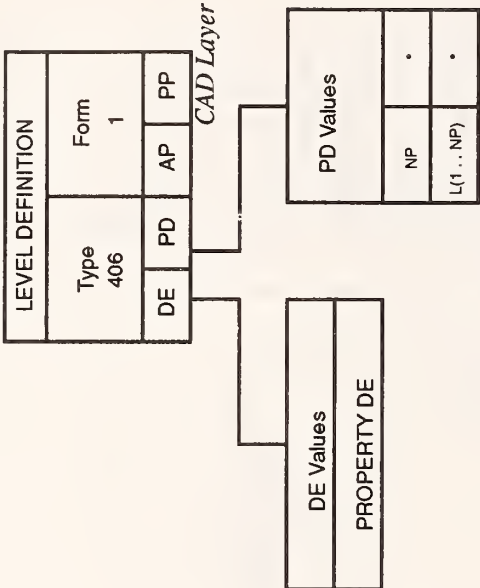
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



5.3.5.3 Line Width Definition

Description:

The Line Width Definition object enables an entity to have specific line width characteristics which include; width, justification, and specific end conditions.

Requirements/Restrictions:

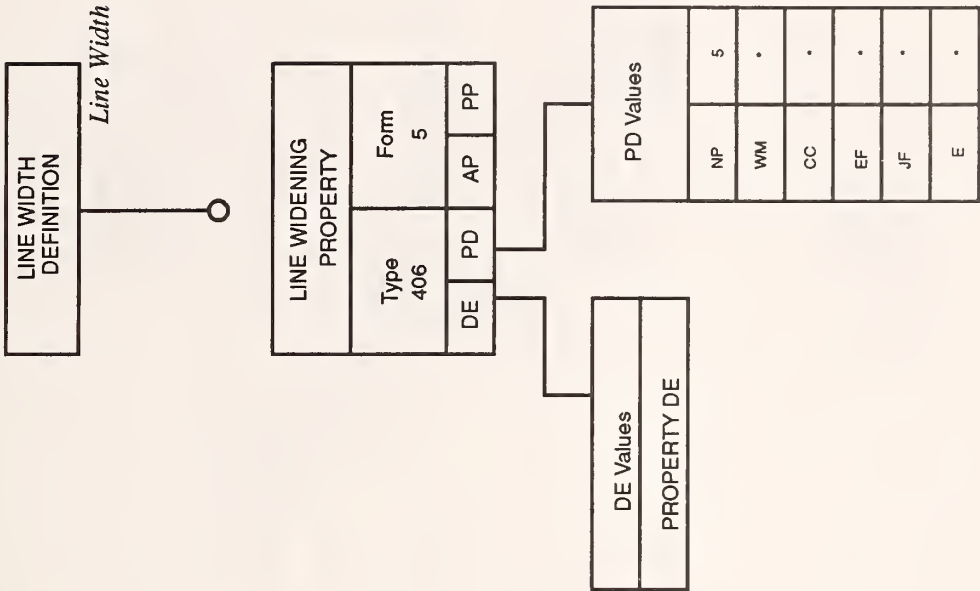
- 1. The Line Width Definition can only be referenced by Display Geometry Objects.

Translation Usage Notes:

General:

Output:

Input:



### 5.3.5.4 Region Fill Definition

#### Description:

The Region Fill Definition object enables a closed curve entity to be displayed with specific fill characteristics (i.e., solid, hatched, etc.).

#### Requirements/Restrictions:

1. The Region Fill Definition can only be referenced by Display Geometry objects which represent closed planar boundaries. Only the following objects can reference a Region Fill Definition.

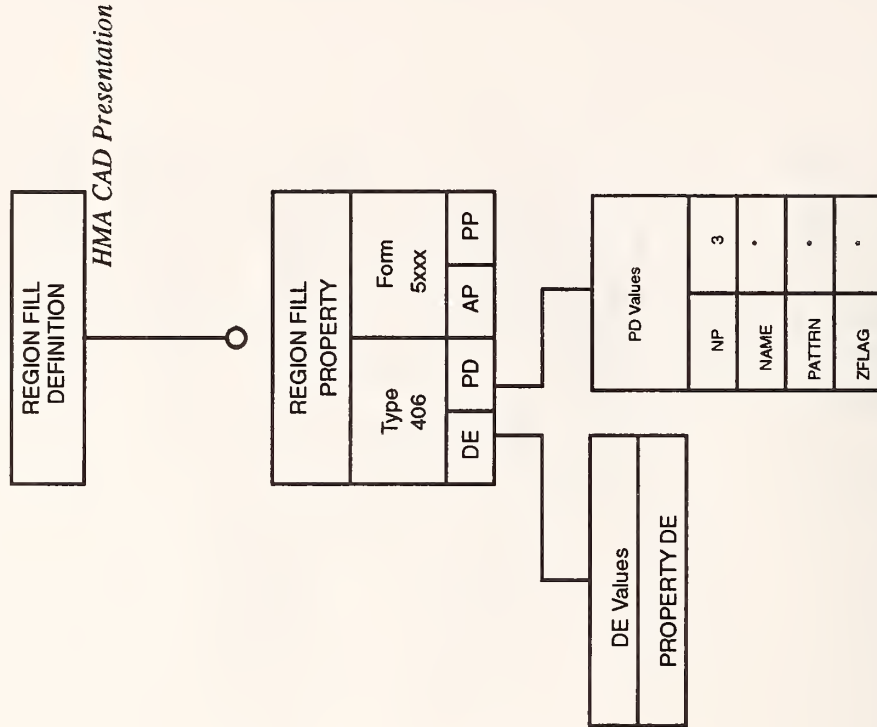
- A) Closed Curve
- B) Predefined Planar Area
- C) Planar Composite Area

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:



A

### 5.3.5.5 Transformation Matrix

**Description:**

The Transformation Matrix object is either a Transformation Matrix (Standard) a Transformation Matrix (Mirrored).

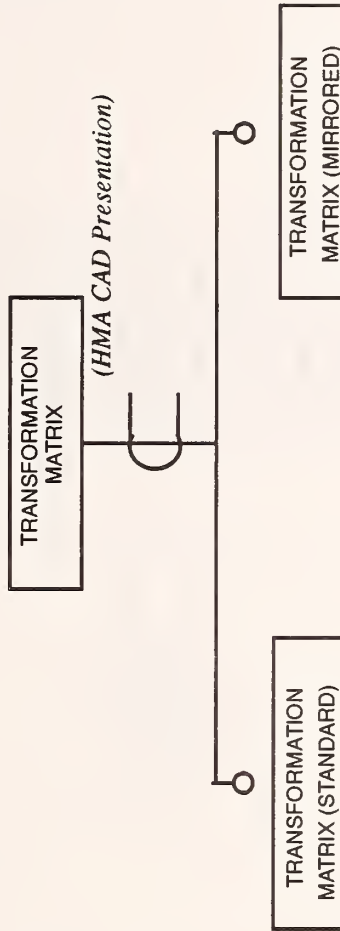
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



### 5.3.5.6 Transformation Matrix (Mirrored)

**Description:**

The Transformation Matrix (Mirrored) object specifies an X,Y,Z rotation and an X,Y,Z offset in a left handed coordinate system.

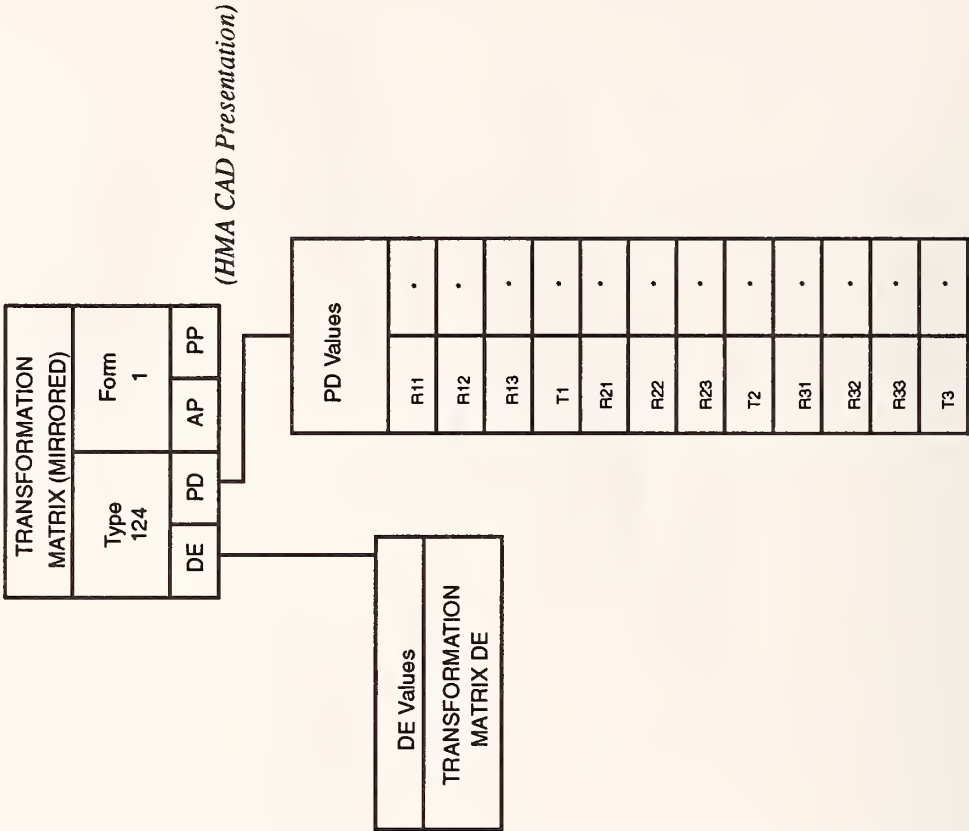
**Requirements/Restrictions:**

**Translation Usage Notes:**

**General:**

**Output:**

**Input:**



5.3.5.7 Transformation Matrix (Standard)

Description:

The Transformation Matrix (Standard) object specifies an X,Y,Z rotation and an X,Y,Z offset in a right handed coordinate system.

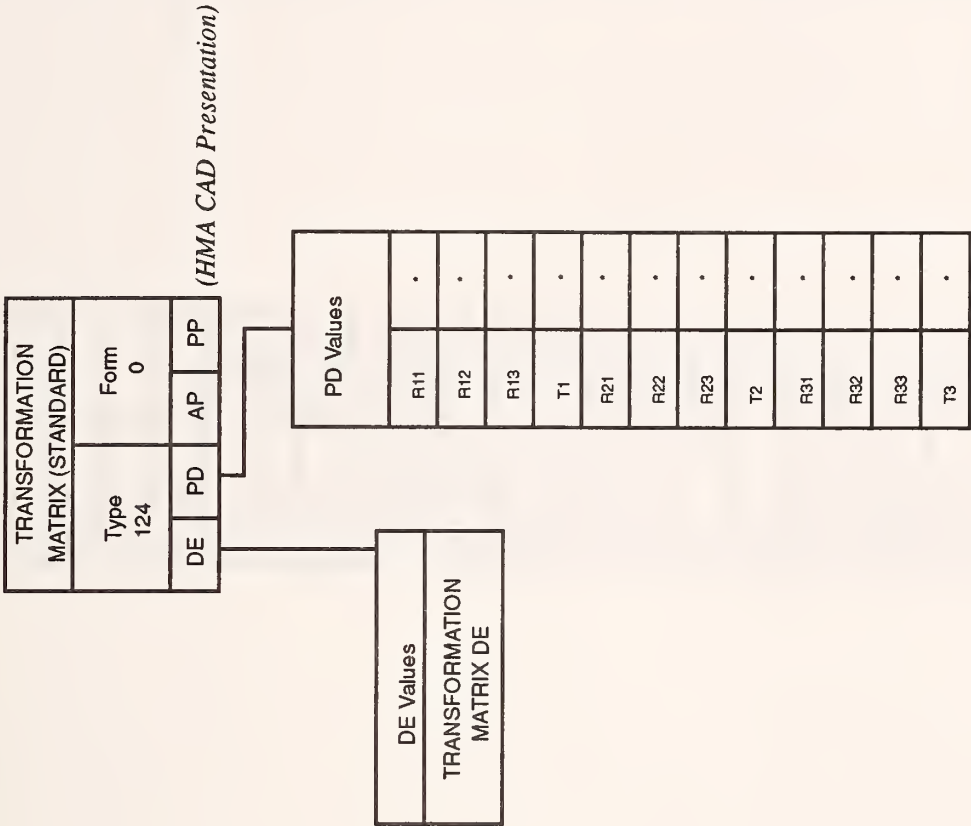
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



## 5.3.6 DE Section Object Models

### 5.3.6.1 Associativity DE

#### Description:

The Associativity DE object is an IGES Directory Entry Section template to be used by all associativity entities.

#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:

## DE Section Object Models

DE Values	
Entity Type	402
Parameters	--
Structure	N/A
Line Font	N/A
Level	N/A
View	N/A
TM	N/A
LDIs Assoc	N/A
Status Number	Blank
	N/A
	Subord
	•
Entity Use	3
Hierarchy	N/A
Sequence	--
Entity Type	402
Line Weight	N/A
Color	N/A
Parm Count	--
Form number	•
Reserved	--
Reserved	--
Label	N/A
Subscript	N/A
Sequence	--

### 5.3.6.2 Color Definition DE

#### Description:

The Color Definition DE object is an IGES Directory Entry Section template to be used by all Color Definition entities.

#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:

DE Values	
Entity Type	314
Parameters	--
Structure	N/A
Line Font	N/A
Level	N/A
View	N/A
TM	N/A
LDIs Assoc	N/A
Status Number	Blank
	Subord
	Entity Use
	Hierarchy
Sequence	--
Entity Type	314
Line Weight	N/A
Color	N/A
Parm Count	--
Form number	0
Reserved	--
Reserved	--
Label	N/A
Subscript	N/A
Sequence	--

### 5.3.6.3 Definition DE

#### Description:

The Definition DE object is an IGES Directory Entry Section template to be used by all definition entities.

#### Requirements/Restrictions:

#### Translation Usage Notes:

#### General:

#### Output:

#### Input:

DE Values	
Entity Type	*
Parameters	--
Structure	N/A
Line Font	N/A
Level	N/A
View	N/A
TM	N/A
LDIs Assoc	N/A
Status Number	Blank
	N/A
	Subord
	*
Entity Use	02
Hierarchy	01
Sequence	--
Entity Type	*
Line Weight	N/A
Color	N/A
Parm Count	--
Form number	*
Reserved	--
Reserved	--
Label	N/A
Subscript	N/A
Sequence	--

5.3.6.4 Geometry DE

Description:

The Geometry DE object is an IGES Directory Entry Section template to be used by all display geometry entities.

Requirements/Restrictions:

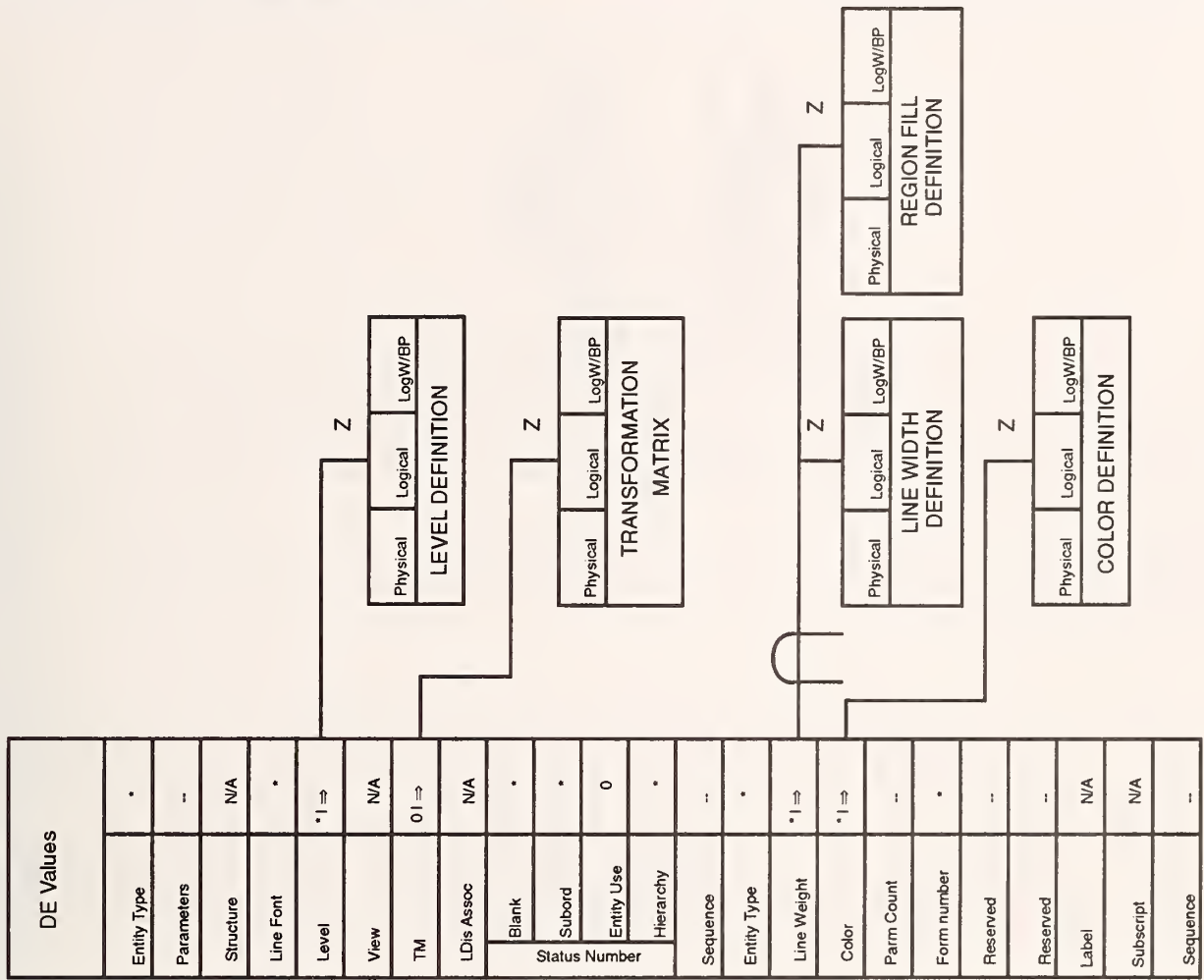
- 1. The Region Fill Definition only applies to the Closed Curve, Predefined Planar Area, and Planar Composite Area objects.
- 2. The Line Width Definition only applies to the Curve, Predefined Planar Area, Planar Composite Area, and Text String objects.

Translation Usage Notes:

General:

Output:

Input:



5.3.6.5 Instance DE

Description:

The Instance DE object is an IGES Directory Entry Section template to be used by all instance entities.

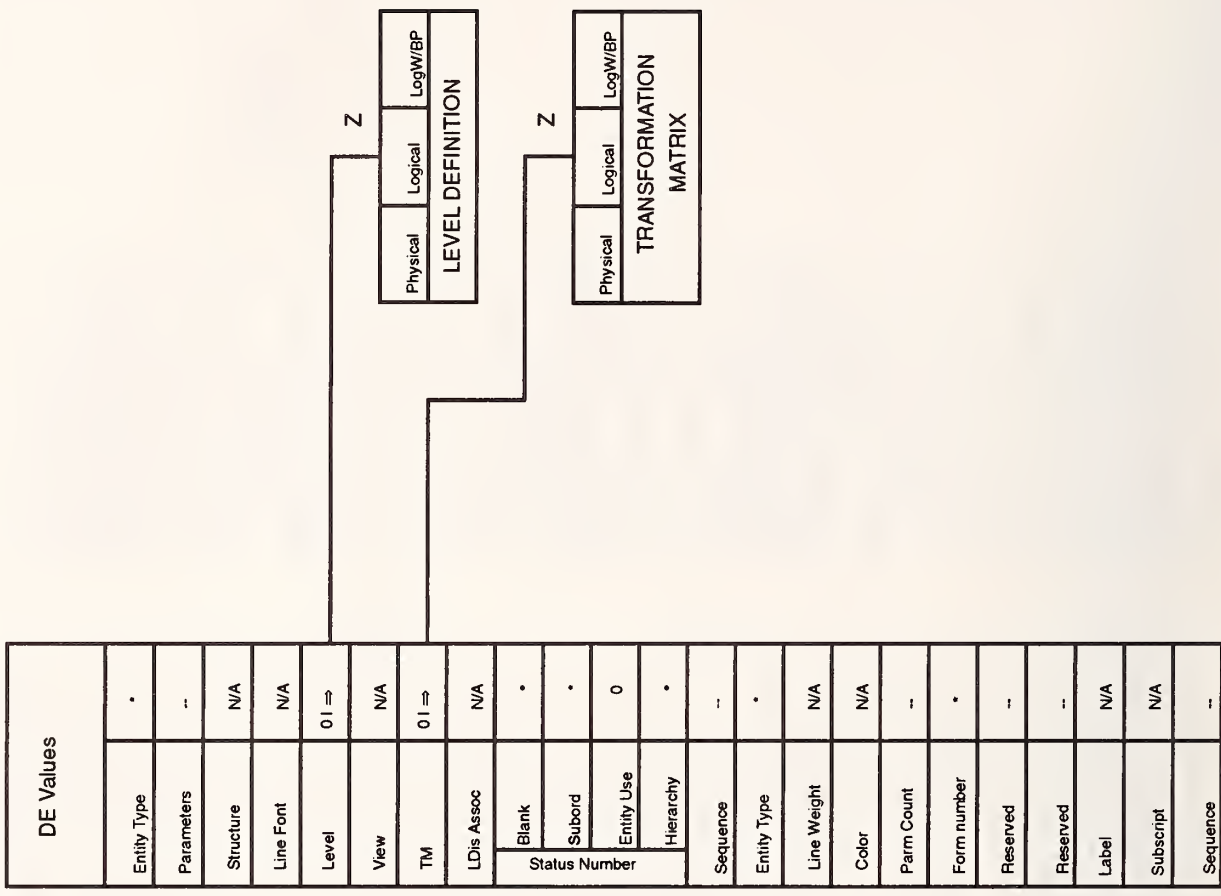
Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:



### 5.3.6.6 Property DE

#### Description:

The Property DE object is an IGES Directory Entry Section template to be used by all property and attribute entities.

#### Requirements/Restrictions:

1. For the Level to LEP Layer Map Property, SUBORD = 0

#### Translation Usage Notes:

##### General:

##### Output:

##### Input:

DE Values	
Entity Type	*
Parameters	--
Structure	N/A
Line Font	N/A
Level	N/A
View	N/A
TM	N/A
LDIs Assoc	N/A
Status Number	Blank
	Subord
	Entity Use
	Hierarchy
Sequence	--
Entity Type	*
Line Weight	N/A
Color	N/A
Parm Count	--
Form number	*
Reserved	--
Reserved	--
Label	N/A
Subscript	N/A
Sequence	--

5.3.6.7 Transformation Matrix DE

Description:

The Transformation Matrix DE object is an IGES Directory Entry Section template to be used by all Transformation Matrix entities.

Requirements/Restrictions:

Translation Usage Notes:

General:

Output:

Input:

DE Values		TRANSFORMATION MATRIX		
Entity Type	124	Physical	Logical	LogW/BP
Parameters	--			
Structure	N/A			
Line Font	N/A			
Level	N/A			
View	N/A			
TM	0 1 =>			
LDIs Assoc	N/A			
Status Number	Blank			
	Subord			
	Entity Use			
	Hierarchy			
Sequence	--			
Entity Type	124			
Line Weight	N/A			
Color	N/A			
Parm Count	--			
Form number	0 1 1			
Reserved	--			
Reserved	--			
Label	N/A			
Subscript	N/A			
Sequence	--			

## 6. IMPLEMENTATION AND CONFORMANCE TESTING GUIDELINES

The successful exchange of information using an IGES AP requires the participating organizations to establish information configuration control and software configuration control procedures for their product data creation and exchange systems. It must be understood that the use of IGES AP's will in many cases require organizations to revise their policies and procedures for the creation, exchange, and archival storage of product data. The successful use of an IGES application protocol also requires that the participating IGES processors conform to the AP specification. The purpose of conformance testing is to increase the confidence that different implementations of the AP will be able to exchange information successfully. This AP requires that the functionality of the hybrid constructs of the ARM be preserved in the translation into and out of the IGES format. Therefore, the CAD system for which the processors are being tested must provide this minimum level of functionality for modeling hybrid systems. In addition, the processors must completely support the functionality defined in the AIM section.

Due to the complexity of this AP, it is not feasible to conduct exhaustive testing of processors for all possible combinations of AP constructs. The conformance testing requirements described in this section cover all constructs of the ARM. The enumerated test groups (sec 6.3) are not exhaustive (i.e., they do not cover all possible combinations of ARM and AIM constructs) although the commonly encountered information required for transfer is present.

### 6.1 PROCESSOR CONFORMANCE REQUIREMENTS

The conformance requirements for implementations of this AP are enumerated as follows: 1.) All IGES files created by an AP compliant preprocessor shall conform to the IGES specification, Version 5.1 and to the constructs specified in this AP. An AP compliant preprocessor shall convert hybrid information of the ARM into the IGES constructs specified in the AIM, with all the required attributes and values. The functionality defined for each construct of the ARM shall be preserved. 2.) An AP compliant postprocessor shall interpret files that conform to the IGES constructs specified in this AP. It shall also convert each construct of the AIM into native constructs which match the geometry, attributes, and relationships of the hybrid constructs specified in the ARM. The functionality of the hybrid constructs shall be preserved.

Development and use of the IGES AP Abstract Test Suite is divided into several Test Groups (TG). Each test group contains discrete Test Purposes (TP). A TP defines the objective of an abstract test case. For a preprocessor, the TP begins with "to test the generation of a(n)...". For a post processor the TP begins with "to test the interpretation of a(n)...". An abstract test case is required for the preprocessor and postprocessor. An abstract test case is derived from a TP and is written in a formal language. When parameter values are provided for the constructs in the abstract case, it can be used to generate an executable test case. An abstract test case contains: TP; test case identifier; reference to specific parts of the AP; definition of constructs required to exercise the TP; statements indicating the construction sequence; and verdict criteria. Abstract test cases are documented in non-system specific procedures and are used to produce comparable results from the conformance testing of multiple implementations.

An executable test case is derived from an abstract test case and is in a form which allows it to be

An executable test case is derived from an abstract test case and is in a form which allows it to be run on the implementation under test. An executable test case contains some or all of the following; TP; test case identifier, reference to specific parts of the AP; constructs required to exercise the TP together with their associated parameter values; a test script defining the construct sequence; verdict criteria; an IGES file for postprocessor conformance testing; and a pictorial representation of the populated constructs.

## 6.2 Test Purposes

The Test Groups in this section each have unique test purposes. The purposes indicated below are general, and are not intended to constrain testing to other possible purposes.

### Test Group 1: Product Drawing

Purposes for this test are to assure that IGES files containing 2-Dimensional drawings can be transferred and both systems participating in the testing produce printed documentation which:

1. contains the identical text, and similar text font, spacing, and text characteristics;
2. contains the same graphics, similar in shapes and appearance, with identical dimensioning numerics, notes text, and waveform and other charted notation labeling;
3. and in general, can be considered equivalent in ability to communicate man-readable product definition for purposes of specification drawings.

### Test Group 2: Photolithography; consisting of numerically-expressed geometry

Purposes for this test are to assure that IGES files containing 2-Dimensional geometry can be transferred and both systems participating in the testing produce photographic artwork which:

1. contains tooling marks (fiducials) which can be superimposed to a visual (unaided) accuracy acceptable for the product type;
2. contains computer-generated feature patterns which match in shape and placement to a visual (unaided) accuracy acceptable for the product type;
3. contains traces which match in width and placement to a visual (unaided) accuracy acceptable for the product type;
4. contains solid-filled areas which match in shape and placement to a visual (unaided) accuracy acceptable for the product type;
5. contains text characters (usually used for part identification/labeling) which are identical in text, and similar in character size and placement acceptable for the product type.

### Test Group 3: Machine Control; parametric data used for numeric control of machine operations

Purposes for this test are to assure that IGES files containing product models can be transferred and both systems participating in the test, which are capable of post-processing information for the same numerically controlled machines, will produce control data that results in the same set of machine actions.

### Test Group 4: CAD System to CAD System Transfer

Purposes for this test is to assure that IGES files can be read by another CAD system with the originating CAD system's non-product attributes retained in the receiving system. All of the contents of Test Groups 1 through 3 are not to be considered in this Test Group. CAD

### 6.3 Enumerated Application Protocol Test Groups

Complete testing to this AP shall consist of testing for each of the test purposes in each of the test groups except for the Technical Illustrations IGES file which will only require Test Group one.

#### Test Group 1: Product Drawing

Requirements for this test are equivalent to the requirements specified for 2-Dimensional drafting application protocols. All entities listed in Display Geometry of section 5 are included for this test case. In the event of conflict in general requirements, such drafting specifications shall take precedence. In addition to general drafting test requirements, the following test sub-groups shall be specifically included.

TG 1.1 Schematic: The details of gate symbols, lines (including bus-lines), signal labels, and miscellaneous symbols found on a schematic graphic.

TG 1.2 Bill of Materials; Tabular information needed for assembly of parts.

TG 1.3 Top Assembly View; includes substrate and component outlines.

#### Test Group 2: Photolithography; consisting of numerically expressed geometry including

TG 2.1 Flashed Pads; location, aperture code, size needed by photoplotter systems

TG 2.2 Trace lines; Inflection point coordinates and width information

TG2.3 Polygon-Bound Area; corner point coordinates and fill information

TG 2.4 Tooling Marks; Shape and centering datum coordinates

TG 2.5 Artwork Text; stroking data for text and line weight

#### Test Group 3: Machine Control; parametric data used for numeric control of machine operations

TG 3.1 Wirebond; end type and location coordinates, assigned net (signal) identification

TG 3.2 Component Pick-and-Place; component centering coordinate, orientation, force and depth

TG3.3 Machine Metrics; machine operational behavior

#### Test Group 4: CAD to CAD Design Presentation Attributes

TG 4.1 CAD Layer assignments; including unrouted signals layer

TG 4.2 CAD Object Display Colors;

TG 4.3 Correspondence Tables;

Table 1: Summary of Data	
Category	Value
Item 1	100
Item 2	200
Item 3	300
Item 4	400
Item 5	500
Item 6	600
Item 7	700
Item 8	800
Item 9	900
Item 10	1000

The following text describes the data presented in the table above. It provides a detailed analysis of the values and their distribution across the different categories. The data shows a clear upward trend, with values increasing from 100 to 1000 across the ten items. This suggests a positive correlation between the item number and the value.

Further analysis of the data reveals that the values are evenly spaced, with a constant difference of 100 between consecutive items. This indicates a linear relationship between the item number and the value. The data is presented in a clear and concise manner, allowing for easy interpretation and understanding.

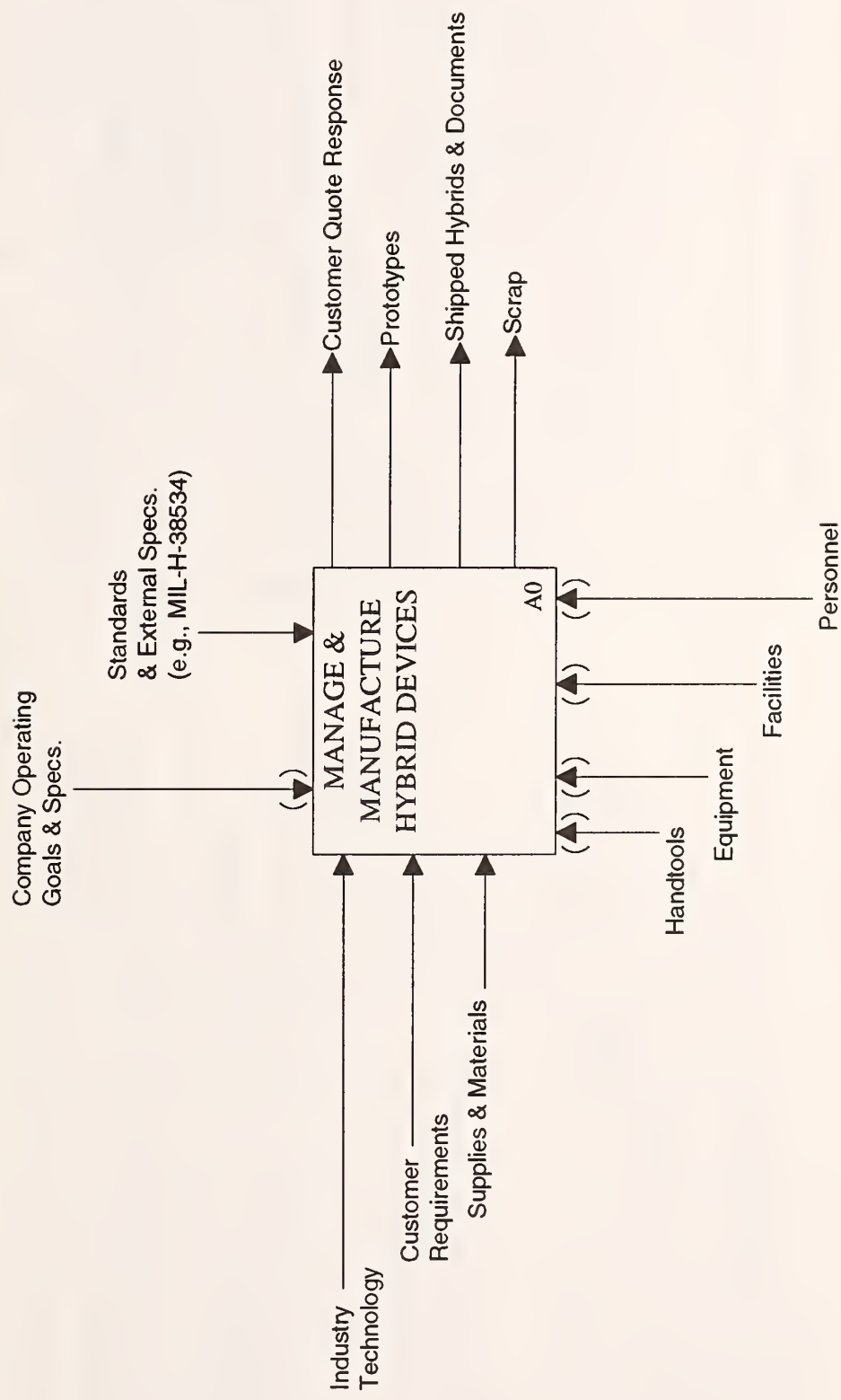
# APPENDIX A. HYBRID APPLICATION ACTIVITY MODEL

## A. ACTIVITY MODEL CONTENTS

A-0	Model Context
A0	Manage and Manufacture Hybrids
A0 Text	Text: Manage and Manufacture Hybrids
A2	Perform Engineering
A2 Text	Text: Perform Engineering
A3	Assure Product Quality
A3 Text	Text: Assure Product Quality
A32	Perform Quality Appraisal
A32 Text	Text: Perform Quality Appraisal
A4	Produce Hybrids
A4 Text	Text: Produce Hybrids
A41	Build Networks
A41 Text	Text: Build Networks
A42	Assemble Devices
A42 Text	Text: Assemble Devices
A43	Test Hybrid
A43 Text	Text: Test Hybrid



USED AT:	AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 10/31/91 REV:	WORKING DRAFT	READER	DATE	CONTEXT: Top
NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
			PUBLICATION			



PURPOSE: To provide the manager with the information context needed for planning automation changes for his hybrid design and fabrication shop.  
The text describing each activity is intended to be generic; it is not meant to be prescriptive or to constrain processes being defined.

VIEWPOINT: The data exchange problem as seen by designers and manufacturers of hybrid microcircuit assemblies.

NODE:	TITLE: APPLICATION PROTOCOL ACTIVITY MODEL	NUMBER:
-------	--	---------



USED AT:	AUTHOR:	Charles Azu	DATE:	10/31/91	WORKING	READER	DATE	CONTEXT:
	PROJECT:	NOSC Hybrid MicroCIM	REV:	4/8/92	DRAFT			
					RECOMMENDED			
					PUBLICATION			
NOTES:		1 2 3 4 5 6 7 8 9 10						

MANAGE & MANUFACTURE HYBRID DEVICES

1. Manage Customer Orders: Orders for hybrid circuits are received in the form of a requirements package. Some manufacturers require only the system definition of the "black box" that they are to design and build (SCD or data equivalent). The orders are analyzed to see if the manufacturing organization has the capability to produce the hybrid circuit. If the organization can produce the hybrid, the customer is given a quote for work. A preliminary schedule is made based on the customer requirements. The schedule along with customer requirements are used as a control and input to the perform engineering activity. Based on the Customer Requirements the applicable Military and Industry Standards and Specifications are chosen for the entire design, engineering, and production process. A Quality Function Deployment (QFD) phase may be entered during this activity. The QFD results can be translated into a type of hybrid at the end of the phase.

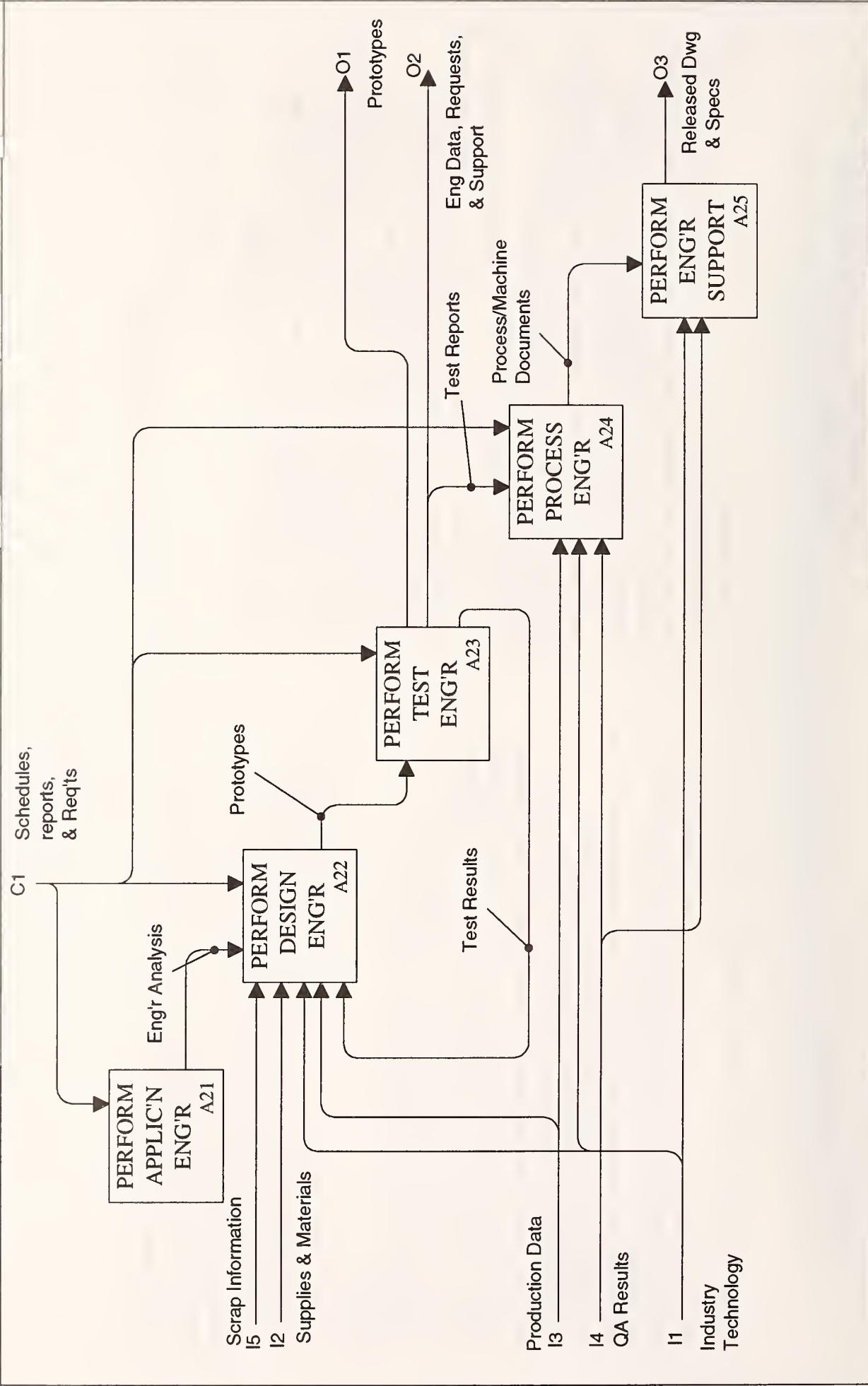
2. Perform Engineering: The engineering of the hybrid circuit takes place using the customer requirements, government & industry standards as guideline for the work done. Availability of supplies, materials, and new technology are taken into consideration during the design of a particular hybrid circuit. During this activity, all the operations take place that transform the customer's requirements into a set of documentation (schematics, netlists, test requirements, layout, etc.) and a released design that will be used to build prototype and production devices.

3. Assure Product Quality: The goal of this activity is to assure that the manufacturer's products meet both customer and government quality requirements. Production data is analyzed in this activity using SPC and design of experiments methodologies. Scrapped products are inspected to find their defects. Results of this activity are fed back to Perform Engineering. A quality plan is formed using cusotmer requirements and it is updated using feedback from production. The quality plan along with inspection results are part of the documentation delivered to the customer.

4. Produce Hybrid: In accordance with released design and specifications from engineering, the hybrids are produced using the supplies and materials. The activity achieves this by planning, directing, and performing production activities that integrate materials, equipment, and personnel, to produce customer shipments. During the production process, some product that doesn't meet quality specifications is scrapped. Production data is taken and kept on hybrids and their processes during production. This data is feedback to engineering and quality assurance. Approved hybrids are packaged and shipped to the customer along with their associated documentation.

NODE:	A0 TEXT	TITLE:	MANAGE AND MANUFACTURE HYBRID DEVICES	NUMBER:
-------	---------	--------	---------------------------------------	---------

USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT:
PROJECT: NOSC Hybrid MicroCIM	REV: 1126/91		DRAFT			<input type="checkbox"/>
NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			<input type="checkbox"/>
			PUBLICATION			<input type="checkbox"/>



NODE: A2	TITLE: PERFORM ENGINEERING	NUMBER:
----------	----------------------------	---------

USED AT:	AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 10/31/91 REV: 4/8/92 6/9/92	WORKING DRAFT RECOMMENDED PUBLICATION	READER	DATE	CONTEXT: Top
NOTES: 1 2 3 4 5 6 7 8 9 10						

## PERFORM ENGINEERING, A2

1. Perform Application Engr.: Part of this activity consists of forming a design team to review the customer requirements to facilitate the hybrid design. A few of the requirements to be reviewed consist of hybrid package size, number of pins, current/voltage limitations, environmental considerations, and testing requirements.
2. Perform Design Engineering: In this activity the design of the hybrid substrate and the fully built up hybrid is accomplished. The substrate design is accomplished with the development of its layout and then its artwork. For the built up hybrid, layouts are developed which are then used to complete the assembly details and generate the masks required for network fabrication. Material requirements for the network and assembly are developed and documented in drawings called bill of materials. The design team reviews the complete hybrid drawings and documentation. The team may run simulations of the circuit on a CAD machine as part of the review effort. The task in this activity is the building of prototype hybrids to prove out the design concepts use in the hybrid design. There is a tight coupling between this activity and Perform Process Engineering.

3. Perform Test Engineering: The purpose of this activity is to develop test systems. The test systems include those associated with electrical testing, active laser trimming, and burning-in-devices. Test systems are built for testing the product as well as the individual components on the hybrid. In conjunction with the development of the test systems, test plans are designed. The prototypes built in the previous activity are tested according to the test plan using the testing systems. Problems encountered in the fabrication or testing of the prototypes lead to modification in the drawings and procedures used to build/test the hybrid. When the prototypes have successfully passed all requirements, they are ready for production.

4. Perform Process Engineering: This activity consists of developing the procedures to produce the number of hybrids required. Results from the prototype hybrid build are used to develop the production processes and set production parameters (ie thru put rate thru a pick & place machine). Current technology and existing equipment are considered in the development of the process. The usual governing factor in developing the process is the number of hybrids of a certain type which will be built. Also taken into consideration are new technological developments. Process documentation is a result of this activity. Feedback from production is also taken in to update and refine the process parameters and documentation. There is a tight coupling between this activity and Perform Design Engineering.

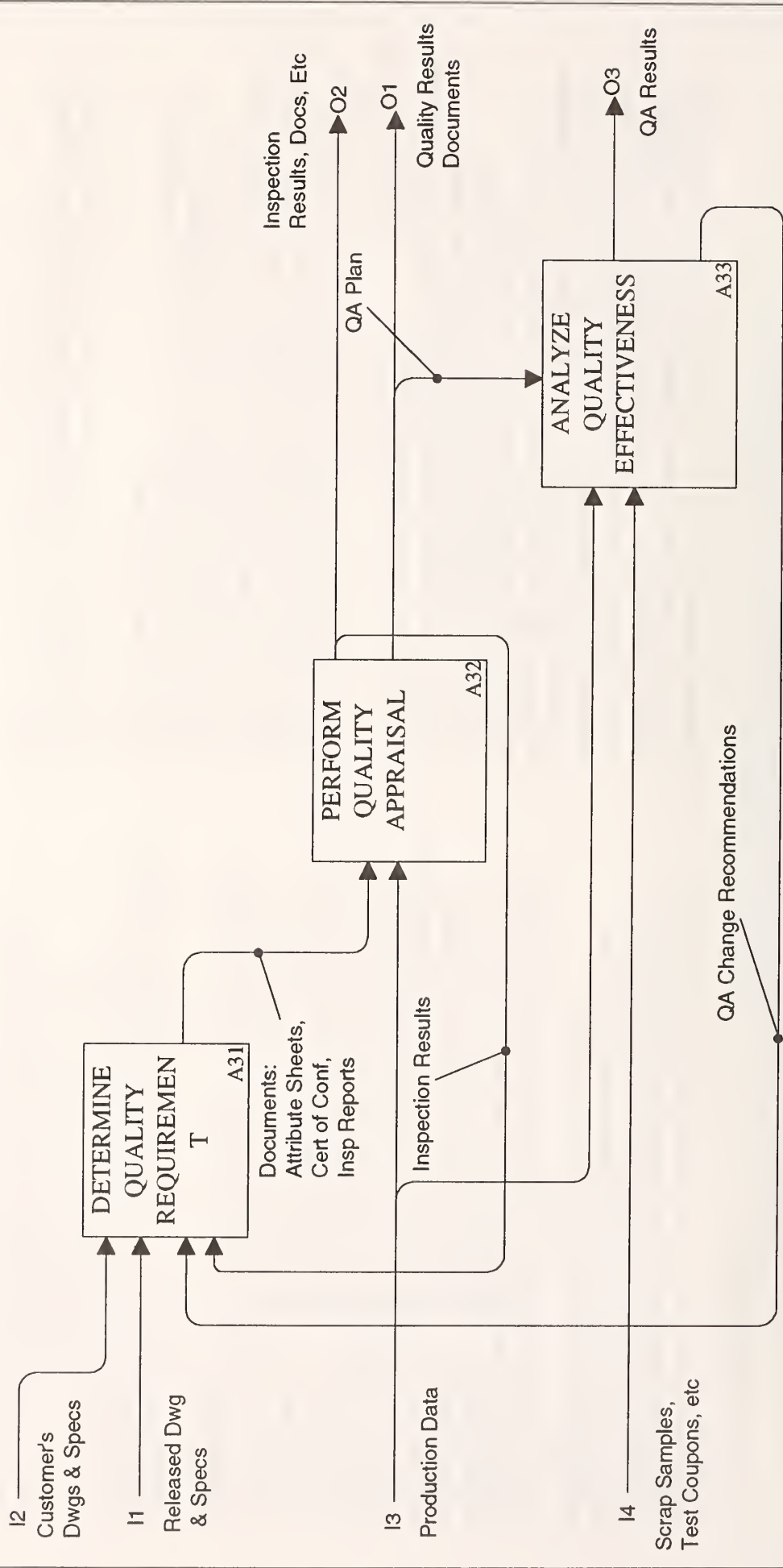
5. Perform Engineering Support: This activity maintains configuration control through a variety of procedures including document control, software control, and change approval control. A vital part of this activity is the continuing support of the product throughout its life cycle. These support activities include: resolving production yield issues, failure analysis, providing the technical interface with customers, serving on the material review board, and developing ongoing product improvements.

NOTE- The Perform Design Engineering and Perform Process Engineering are co-mingled in many organizations as part of a Concurrent Engineering program. The two processes can and often do run in parallel.

NODE: A2 TEXT	TITLE: PERFORM ENGINEERING
---------------	----------------------------

NUMBER:

USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT: <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/>
	PROJECT: NOSC Hybrid MicroCIM	REV:	DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			
			PUBLICATION			



NODE: A3	TITLE: ASSURE PRODUCT QUALITY	NUMBER:
----------	-------------------------------	---------

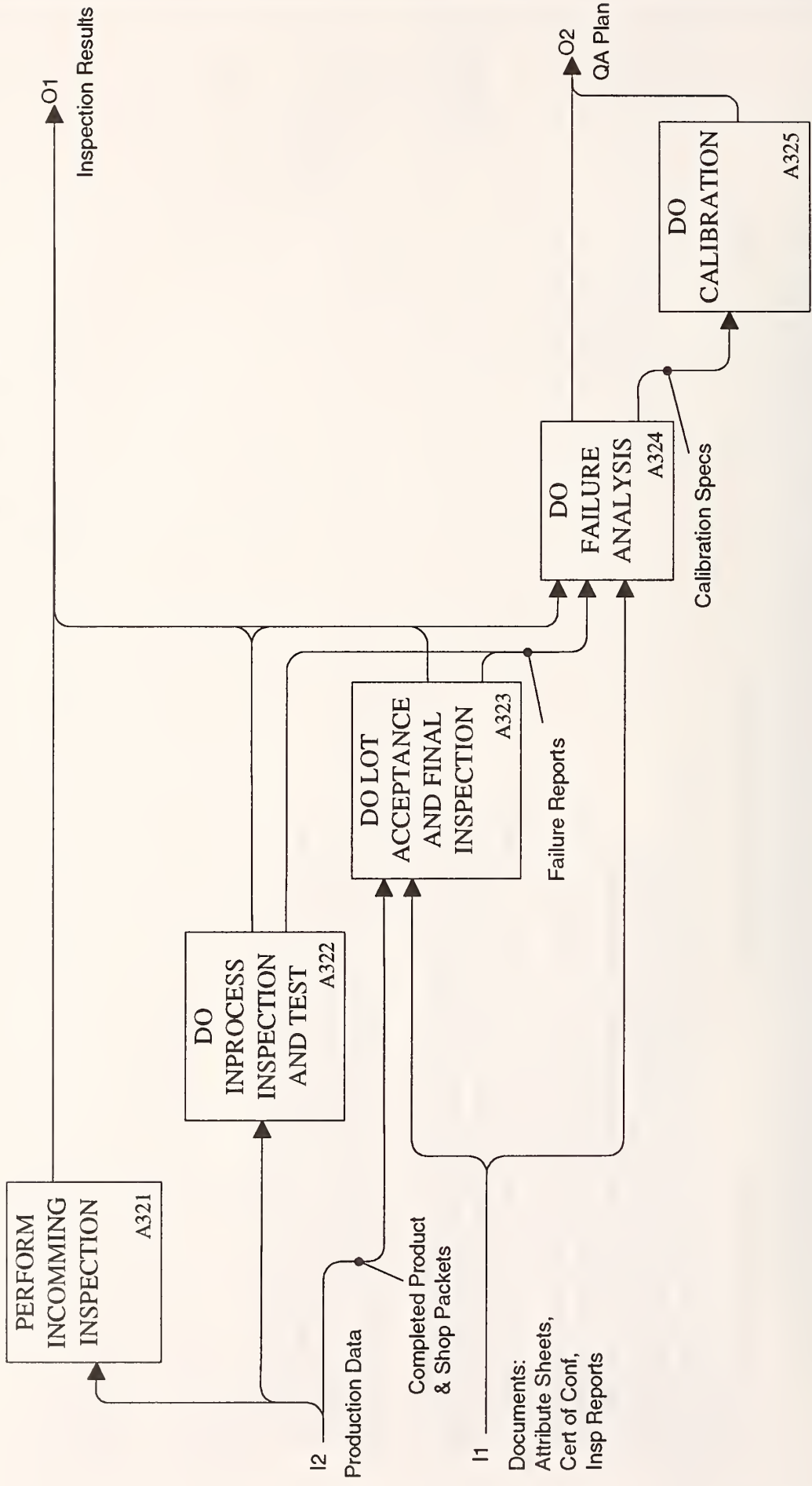
USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT:  Top
	PROJECT: NOSC Hybrid MicroCIM	REV: 4/8/92	DRAFT			
			RECOMMENDED			
			PUBLICATION			
NOTES: 1 2 3 4 5 6 7 8 9 10						

ASSURE PRODUCT QUALITY

1. Determine Quality Requirements: Based on the drawings and engineering data on the hybrid, and the customer requirements for quality and reliability, the quality assurance plan for the hybrid production are established. The quality plans are put in place for implementation on a factory wide basis as the hybrid is moved into production. The company's internal quality plans form part of the overall plan.
2. Perform Quality Appraisals: Inspect/Audit manufacturing and quality (area and process) periodically to assure continued conformance to internal and customer specification requirements. Results from this activity may be used in a continuous process of refining quality plans.
3. Analyze Quality Effectiveness: The quality program is analyzed for its effectiveness. Part of this analysis consists of verifying that the process and testing equipment used in the production of hybrids are properly calibrated and are functioning correctly. Records are kept on calibrations and other adjustments to the equipment.

NODE:	A3 TEXT	TITLE:	ASSURE PRODUCT QUALITY	NUMBER:
-------	---------	--------	------------------------	---------

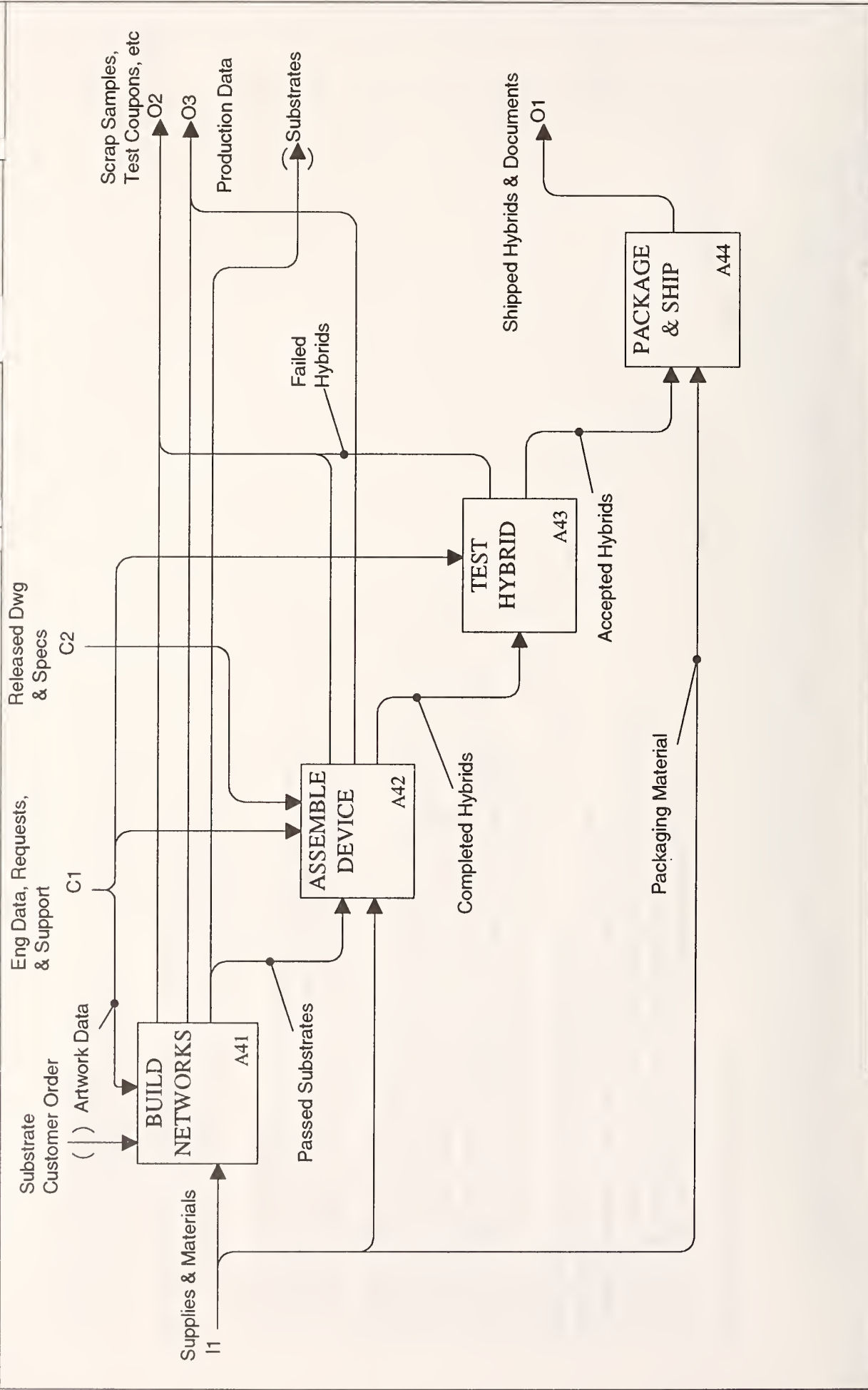
USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT: <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/>
	PROJECT: NOSC Hybrid MicroCIM	REV:	DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			
			PUBLICATION			



NODE: A32	TITLE: PERFORM QUALITY APPRAISAL	NUMBER:
-----------	----------------------------------	---------

USED AT:		AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 10/31/91 REV: 4/8/92	WORKING DRAFT RECOMMENDED PUBLICATION	READER	DATE	CONTEXT: Top
		NOTES: 1 2 3 4 5 6 7 8 9 10					
PERFORM QUALITY APPRAISAL							
<p>1. Perform Incoming Inspection: Parts and materials needed to build a hybrid are checked for compliance to standards specified by Engineering. An implicit part of this activity is supplier qualification, where the supplier is qualified based upon the results of incoming inspection of the supplier's product. Results of this process are passed supplies, failed supplies, and a supplier qualification report.</p> <p>2. Inprocess Inspection and Test: Substrates and plated hybrids may be periodically checked for compliance to standards during production. The method and amount of inspection is established in the quality plan. Inspection mostly consist of visual and electronic. Product that fails this activity may be either reworked or scrapped. Some supplier qualification is done in this activity and this is feedback to the Perform Incoming Inspection process.</p> <p>3. Final Inspection &amp; Lot Acceptance: This activity consists of a final visual inspection of the built up hybrid before capsulization. Successfully passed hybrids become part of a lot which is accepted for packaging and shipment.</p> <p>4. Failure Analysis: Rework of failed hybrids and substrates is done in this activity. Those hybrids which can not be diagnosed on the shop floor repair area may be taken to engineering for analysis.</p> <p>5. Calibration: Calibration of equipement may occur based on the results of the failure analysis, otherwise calibration is done as part of Analyze Quality Effectiveness.</p>							
NODE: A32 TEXT		TITLE: PERFORM QUALITY APPRAISAL				NUMBER:	

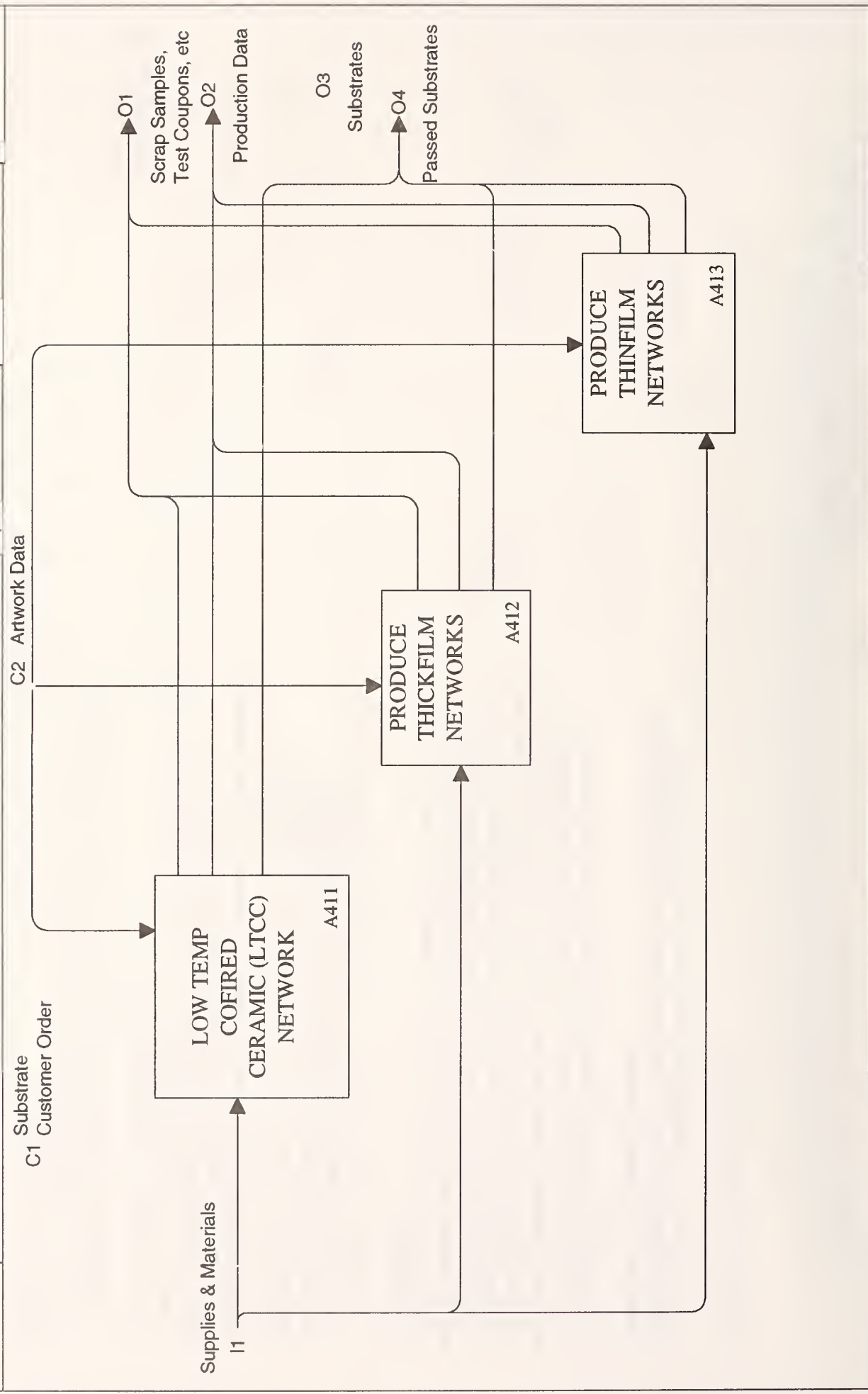
USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT:
PROJECT: NOSC Hybrid MicroCIM	REV: 2/13/92		DRAFT			<input type="checkbox"/>
NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			<input type="checkbox"/>
			PUBLICATION			<input type="checkbox"/>



NODE: A4	TITLE: PRODUCE HYBRIDS	NUMBER:
----------	------------------------	---------

USED AT:	AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 10/31/91 REV: 4/8/92 6/9/92	WORKING DRAFT RECOMMENDED PUBLICATION	READER	DATE	CONTEXT: Top
NOTES: 1 2 3 4 5 6 7 8 9 10						
PRODUCE AND TEST HYBRID (A4)						
<p>1. Build Substrate: Hybrid substrates can be built using one of several methods including thick film, thin film, and green tape. Each method requires different technology and processing.</p> <p>2. Build Hybrid: In this step, the raw materials are transformed, in accordance with the design, into an HMA. The fabrication of an HMA consists of a sequence of fabrication steps such as screenings and firing of conductors and resistor geometries, application of applied devices and components, die and wire bonding, packaging, and various inprocess inspection steps. During the fabrication of the HMA, there may be tests performed (both physical and electrical) to ensure conformance to the tolerance specified in the design. Test results may be used to indicate inprocess corrections for successive devices to be fabricated.</p> <p>3. Test Hybrid: Testing of fabricated components and assemblies consists of two types; testing electrical reliability and screening tests for thermal and mechanical failures. The test for electrical reliability include a pre-seal, pre burn, post burn-in, and a final acceptance test. Electrical tests confirm that all connections have been successfully made and that the circuit meets functional performance requirements. The screens for thermal/mechanical failures include a stabilization bake, temperature cycling, constant acceleration, and leak tests. Hybrids which are rejected from this activity are sent to be reworked. Any need for production improvement as a result of this process is feedback to the Build Hybrid (A42).</p> <p>5. Package and Ship Hybrid Device: This section is shown for completeness. The delivery process may involve packaging, ensuring that documentation is complete, and shipping. This data exists to the extent that it can be obtained from the automation data.</p>						
NODE: A4 TEXT	TITLE: PRODUCE HYBRID					NUMBER:

USED AT:	AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 10/31/91 REV:	WORKING DRAFT RECOMMENDED PUBLICATION	READER	DATE	CONTEXT: <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
NOTES: 1 2 3 4 5 6 7 8 9 10						



NODE: A41	TITLE: BUILD NETWORKS	NUMBER:
-----------	-----------------------	---------

USED AT:	AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 2/13/92 REV: 4/8/92	WORKING DRAFT RECOMMENDED PUBLICATION	READER	DATE	CONTEXT: Top
NOTES: 1 2 3 4 5 6 7 8 9 10						

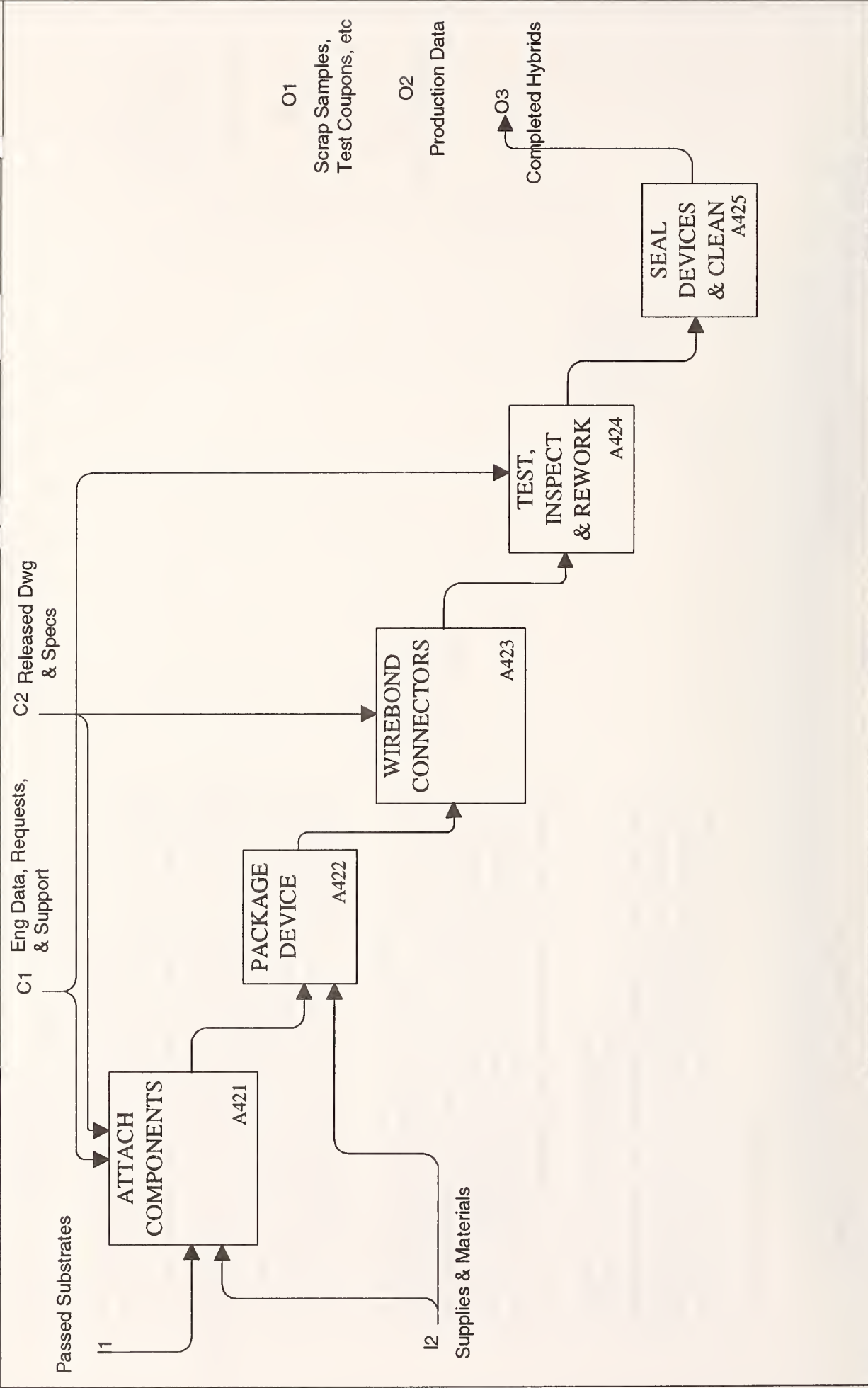
A41 BUILD NETWORKS

1. Hi/Low Temperature Co-fired Ceramics: Also called "green" tape, this substrate type is processed so that the individual layers of a multilayer substrate can be produced separately. The various layers are then laminated together in a stack and fired. Co-fired ceramics are used to fabricate high-density thick film multilayer substrates and packages.
2. Thick Film Networks: These networks are fabricated sequentially. The process involves using screen printing techniques to apply thick film conductors as well as resistive and dielectric pastes. After each screen printing pass (to apply a pattern of thick film material) the substrate is dried and fired at elevated temperatures to convert the film paste to a film with the required electrical and mechanical properties. A substrate usually goes through several passes to deposit all layers.
3. Thin Film Networks: These networks are fabricated using vacuum vapor deposition, sputter deposition, and electroplating to establish conductor and resistor metals. Photoplotting and chemical etching are used to define conductor, resistor, and polyamide geometries. Patterns are formed onto the substrate using precision photolithography. This process involves applying the photoresist, exposing the mask, developing the photoresist. The circuits are baked at elevated temperature to stabilize resistor characteristics, relieve conductor stress, and polymerize the polyamide film. The annealed networks are then resistor trimmed and broken into individual networks.

NOTE: For a particular HMA design, only one of these processes is invoked.

NODE: A 41 TEXT	TITLE: BUILD NETWORKS	NUMBER:
-----------------	-----------------------	---------

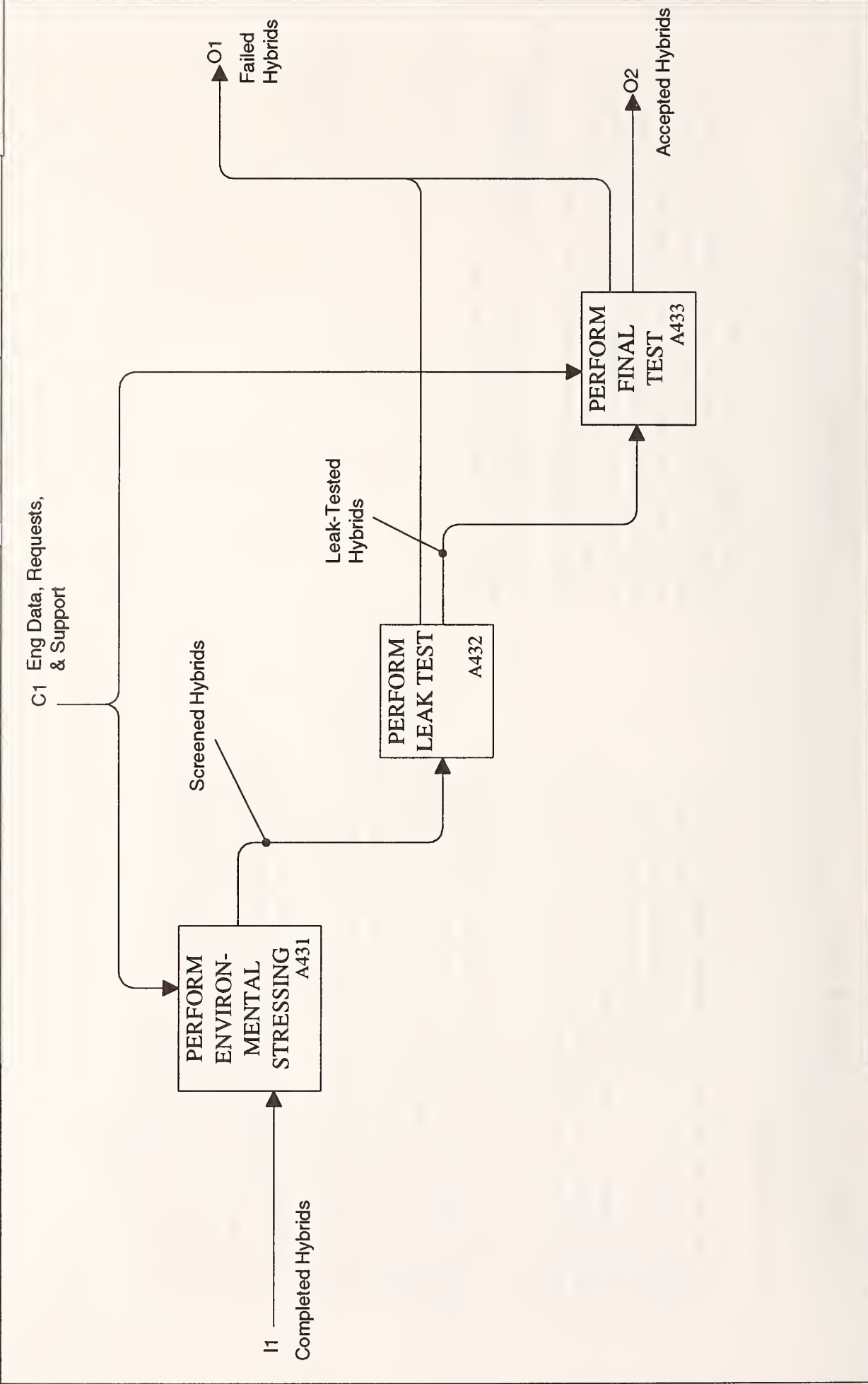
USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT:
PROJECT: NOSC Hybrid MicroCIM	REV:		DRAFT			<input type="checkbox"/>
NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			<input type="checkbox"/>
			PUBLICATION			<input type="checkbox"/>



NODE: A42	TITLE: ASSEMBLE DEVICE	NUMBER:
-----------	------------------------	---------

USED AT:		AUTHOR: Charles Azu		DATE: 2/13/92		WORKING		READER		DATE		CONTEXT:	
PROJECT: NOSC Hybrid MicroCIM		REV: 4/8/92		DRAFT		RECOMMENDED						Top	
NOTES: 1 2 3 4 5 6 7 8 9 10													
<p>A42 Assemble Devices</p> <p>1. Attach Components: Elements such as silicon dies, capacitors, and resistors are attached to the network using appropriate epoxy, eutectic alloy, or solder. The epoxy is often screen printed onto the substrates. Elements are usually attached with pick and place robots. The elements are usually cleaned first. Once all elements are attached to the substrate, the substrate is baked at high temperature to cure the epoxy. This process may be done after the device is packaged depending upon a particular design and a company's methods.</p> <p>2. Package Devices: The assembly networks are packaged into cases and attached with epoxy. The process contains several steps: cleaning the case, epoxying the network to the package, baking the packaged device to cure the epoxy, marking the package with the necessary information for identification, and baking the package and device once more to cure the markings. This process may be done before the components are attached depending upon a particular design and a company's methods.</p> <p>3. Wire Bond Connections: The packaged device is electrically connected to its elements and casing by wire bonds. The hybrid is first plasma cleaned to remove any residue. Second the wire bond connections are made between substrate pads and components. Third the wire bond connections are made between substrate and the leads of the case. These wire bond operations can be performed by an automatic wire bonder.</p> <p>4. Test, Inspect, &amp; Rework: After the hybrid has been wire bonded, the device must be bond pull tested usually with an automatic wire bond pull tester. The device is then electrically tested to insure that all connections have been made and that the device is functioning correctly. The hybrid is visually inspected to insure quality. Hybrids which are rejected during testing or inspection are reworked. Also, some active trimming and tuning of a device is done as a result of electrical test.</p> <p>5. Seal Devices: Hybrid devices are hermetically sealed by welding a cover onto the device. Once the device is sealed, leads preform test/inspection is performed.</p>													
NODE: A 42 TEXT		TITLE: ASSEMBLE DEVICES		NUMBER:									

USED AT:	AUTHOR: Charles Azu	DATE: 10/31/91	WORKING	READER	DATE	CONTEXT: <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
	PROJECT: NOSC Hybrid MicroCIM	REV:	DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10		RECOMMENDED			
			PUBLICATION			



NODE: A 43	TITLE: TEST HYBRID	NUMBER:
------------	--------------------	---------

USED AT:	AUTHOR: Charles Azu PROJECT: NOSC Hybrid MicroCIM	DATE: 2/13/92 REV: 4/8/92	WORKING DRAFT RECOMMENDED PUBLICATION	READER	DATE	CONTEXT: Top
<p>A43 Test Hybrid</p> <p>During this activity the hybrids are passed through environmental screening which include nitrogen bake, temperature cycling, and constant acceleration. The second part of the activity involves testing the hybrid for leaks by pressurizing the device and monitoring for leaks. The final test is burn-in which removes infant mortality. Hybrids which successfully pass these tests are moved to shipping. Those that fail are sent to rework. Some manufacturers perform final electrical test then leak test. Manufacturers do this, despite the violation of Mil-Spec, because HMAs often fail more in electrical test than during leak test.</p>						
NODE: A43 TEXT	TITLE: TEST HYBRID					NUMBER:



## APPENDIX B

### TECHNICAL DISCUSSIONS

#### B.1. A Primary Parent for the ARM

View 4-1 contains seven independent entities, as opposed to most models which have a single independent entity. The multiple independent entity situation was recognized in the early STEP modeling, with one of these models proposing the Enterprise as the single independent parent. The MicroCIM team has discussed adding such an entity, however did not do so because the scope defined for the model does not require such a model refinement. It was recognized that each ARM independent entity employs "ID" in the key. ID is defined in the section 3 Glossary to include data which uniquely identifies the source or owning enterprise. Thus an Enterprise parent is implied.

#### B.2. Netlist Information

The Net entity on ARM View 4-3 has been recognized as *derived* information. Typically the Net consists of a Signal Name with the Reference Designators and Pin Numbers to be associated (i.e., connected) with that signal. The source of Net information is the functional design of the circuitry as presented by a schematic. The Schematic in any particular product design may have been "back-annotated" with net list information from the package design. The Schematic entity itself has not been decomposed into its fundamental entities in this version of the ARM.

#### B.3. Multiple Planning for a Product

The association of Process information with the Product model presents a problem when "re-planning" takes place. This would occur if the product is not completely processed to a single process definition (e.g., second sourcing or reprourement). The team view is that the model provides a place for a particular user to record his planning information. Should the Product data be relocated, the site-specific planning would not be populated, and may be re-defined at the next cite.

#### B.4. Producibility Feedback

The use of "producibility" data in a concurrent engineering situation requires much more attention. As yet the team has discovered no commonly agreed to model of how things like "cost penalties for non-standard designs" or "more easily manufactured trade-offs" are to be placed into a database which engineering could access during layout. These sorts of dispositions seem to take place during "producibility reviews" which requires the knowledge of experienced operations people. As a starting point for capturing such information, several kinds of Rules have been included in the ARM.

#### B.5. Quality

Much of the Application Activity Model (AAM) has been reworded and modified to reflect the use of Total Quality Management (TQM) and Quality Function Deployment (QFD) being practiced. The team expects new attributes will be required for some of the ARM entities.



# NIST Technical Publications

## Periodical

---

**Journal of Research of the National Institute of Standards and Technology**—Reports NIST research and development in those disciplines of the physical and engineering sciences in which the Institute is active. These include physics, chemistry, engineering, mathematics, and computer sciences. Papers cover a broad range of subjects, with major emphasis on measurement methodology and the basic technology underlying standardization. Also included from time to time are survey articles on topics closely related to the Institute's technical and scientific programs. Issued six times a year.

## Nonperiodicals

---

**Monographs**—Major contributions to the technical literature on various subjects related to the Institute's scientific and technical activities.

**Handbooks**—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

**Special Publications**—Include proceedings of conferences sponsored by NIST, NIST annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

**Applied Mathematics Series**—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

**National Standard Reference Data Series**—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a worldwide program coordinated by NIST under the authority of the National Standard Data Act (Public Law 90-396). NOTE: The Journal of Physical and Chemical Reference Data (JPCRD) is published bi-monthly for NIST by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements are available from ACS, 1155 Sixteenth St., NW., Washington, DC 20056.

**Building Science Series**—Disseminates technical information developed at the Institute on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

**Technical Notes**—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NIST under the sponsorship of other government agencies.

**Voluntary Product Standards**—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The standards establish nationally recognized requirements for products, and provide all concerned interests with a basis for common understanding of the characteristics of the products. NIST administers this program in support of the efforts of private-sector standardizing organizations.

**Consumer Information Series**—Practical information, based on NIST research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

Order the **above** NIST publications from: Superintendent of Documents, Government Printing Office, Washington, DC 20402.

Order the **following** NIST publications—FIPS and NISTIRs—from the National Technical Information Service, Springfield, VA 22161.

**Federal Information Processing Standards Publications (FIPS PUB)**—Publications in this series collectively constitute the Federal Information Processing Standards Register. The Register serves as the official source of information in the Federal Government regarding standards issued by NIST pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

**NIST Interagency Reports (NISTIR)**—A special series of interim or final reports on work performed by NIST for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Service, Springfield, VA 22161, in paper copy or microfiche form.

**U.S. Department of Commerce**  
National Institute of Standards and Technology  
Gaithersburg, MD 20899

**Official Business**  
Penalty for Private Use \$300

